EMI-EMC Theory and Troubleshooting

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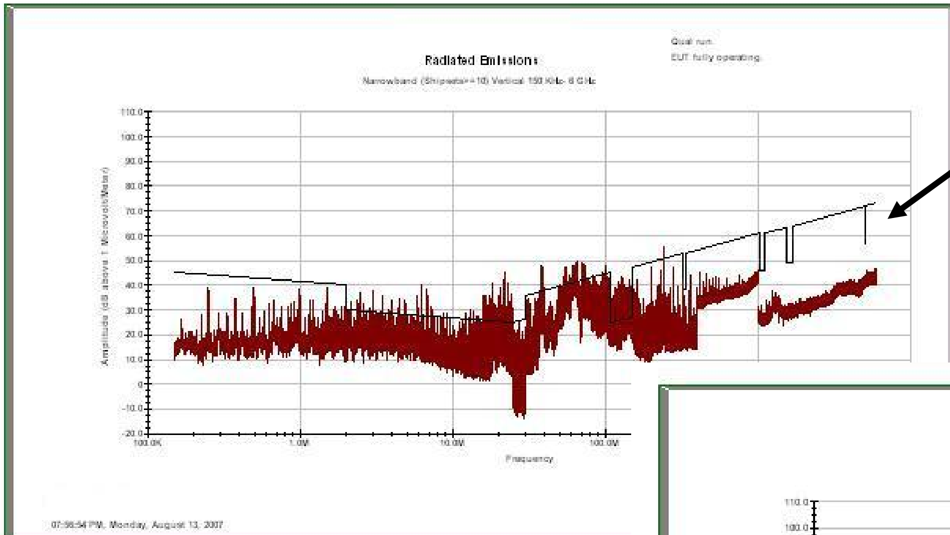
Key Points

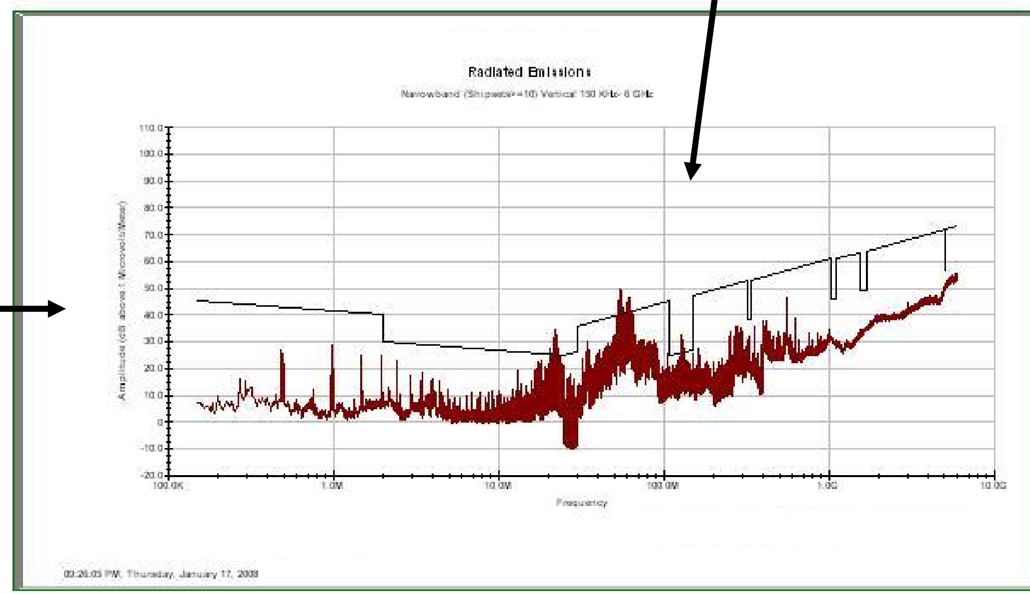
- “Right the First Time” is an optimum way to design equipment
- Avoiding problems requires insight and planning
- Front-end design requires modeling and simulation
- EMI-EMC is getting harder to do because of faster ICs
- Advanced bypassing techniques are needed for PI and I/Os
- Advanced crosstalk control eliminates split planes
- EMI-EMC insight is enabled by advanced computational tools
- Verify your assumptions with measurements and simulations
- Experience and reflection improve insight, foresight, and skill

Partial Redesign of a Microprocessor Board



Original Board

Redesigned Board



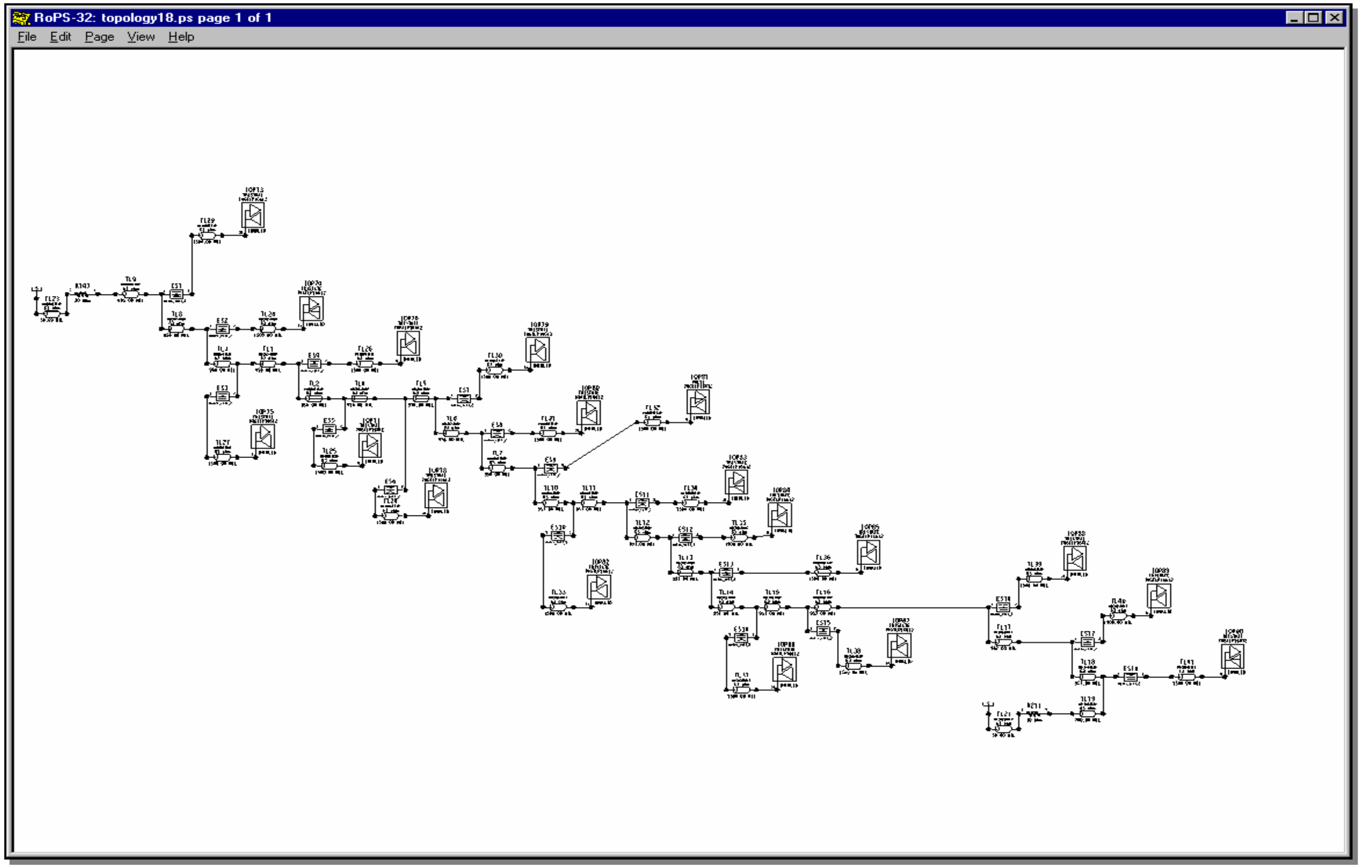
•***What was done:*** Clock nets were simulated and terminated. Floating planes were grounded and layout improved. *Result.*

•***What was missed:*** elimination of moats and splits, proper bypassing, and replacement of single, unshielded connector for all I/Os.

Do you think more could have been accomplished?

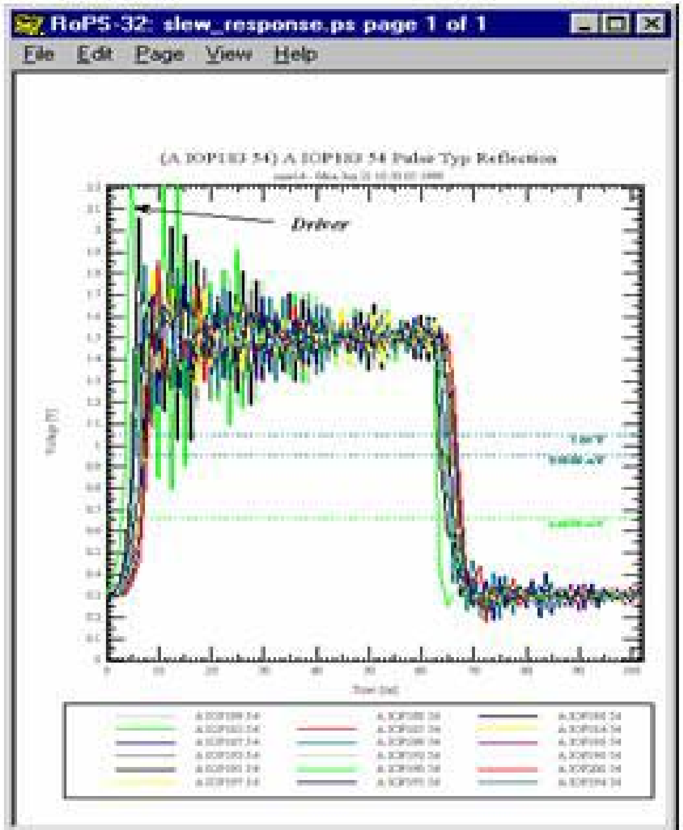
Complexity versus Simplification in Modeling & Simulation

An Example of a Complex Network



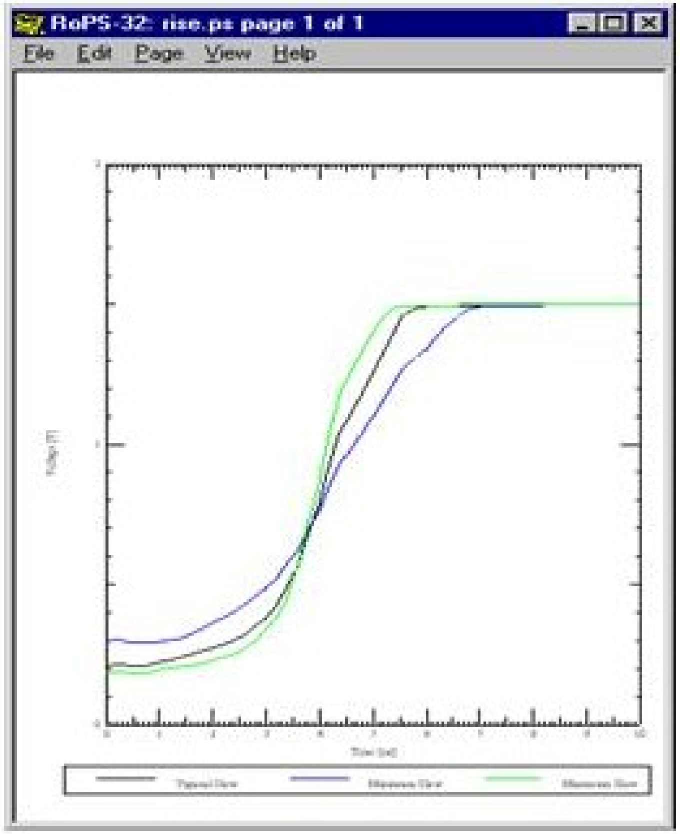
An 18-Slot Bi-Directional Backplane Bus. Courtesy of 3Com. Used with permission

Simulation Results from too Simple a Model



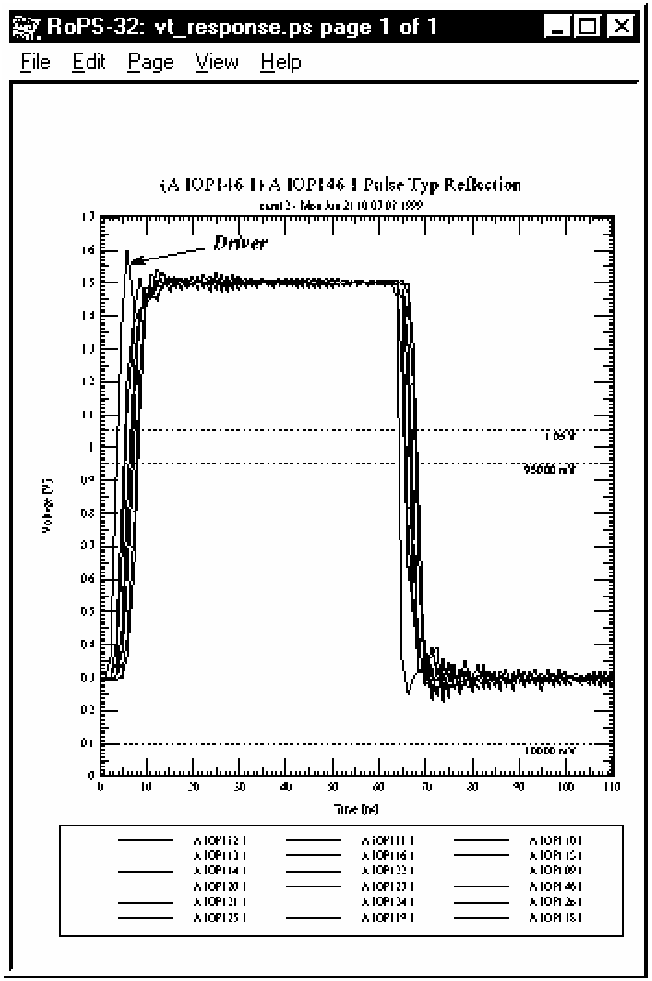
- Complex nets are hard to terminate and have many reflections
- Simple dV/dt modeling and device behavior is inadequate for accurate results
- V-T curves need to be modeled for correct results in GTL/GTLP busses

IBIS Modeling of V-T Curves: How GTLP Drivers Really Behave



- This slide shows how to correctly model GTL/GTLP
- Soft turn-on/turn-off removes many high-frequency components (think about Fourier transformation) from driving the line
- The results of the change in modeling detail are shown next:

Better Models Give Better Results



"Everything should be as simple as possible *and no simpler*."

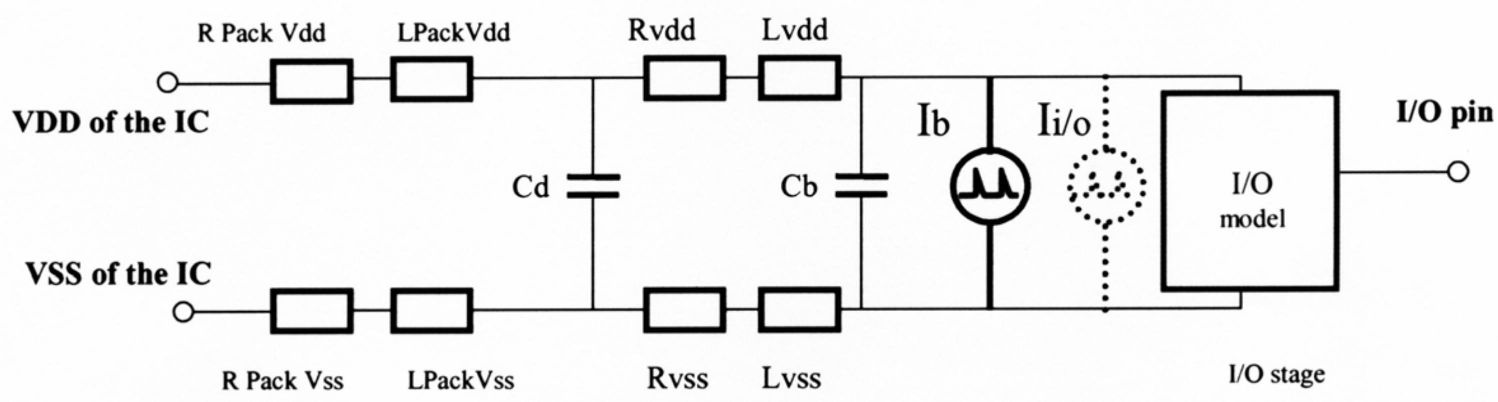
—Albert Einstein

Semiconductor Technology Roadmap

Year	2000	2003	2007	2010	2013
Technology	0.18µm	90nm	65nm	45nm	30nm
Supply Voltage	1.9V	1V	0.7V	0.5V	0.3V
Max area (mm2)	20x20	22x22	25x25	30x30	30x30
Interconnect Layers	6	6-10	6-11	8-12	8-12
CPU clock Frequency [MHz]	800	3000	3500	10,000	25,000
Max N° of Pads	1500	2200	3500	6000	10,000
Interconnections	Tu/Alu/	Cu	Cu	Cu	Cu
Electromagnetic Compatibility					
Conducted emission (µV)	70	90	95	100	100
Measurement methods	TEM, 1ohm	GTEM, 1ohm	GTEM	xGTEM	xGTEM
Frequency range of interest: DC to	1GHz	3GHz	10GHz	30GHz	80GGHz
Conducted susceptibility (A)	30mA	10mA	5mA	1mA	1mA
Radiated susceptibility (V/m)	10	30	50	70	100
Measurement methods	BCI, DPI	xBCI, DPI, GTEM, onchip	xBCI, GTEM, onchip	xGTEM, onchip	xGTEM, onchip
I/O modeling	Ibis v2	Ibis v3	Ibis-ml	unknown	unknown
Core modeling	IMIC	ICEM	ICEM UHF	ICEM xHF	ICEM xHF

- **Slide courtesy of Etienne Sicard, University of INSA-Toulouse. Used with permission**

PI and the IEC 62014-3 Proposal

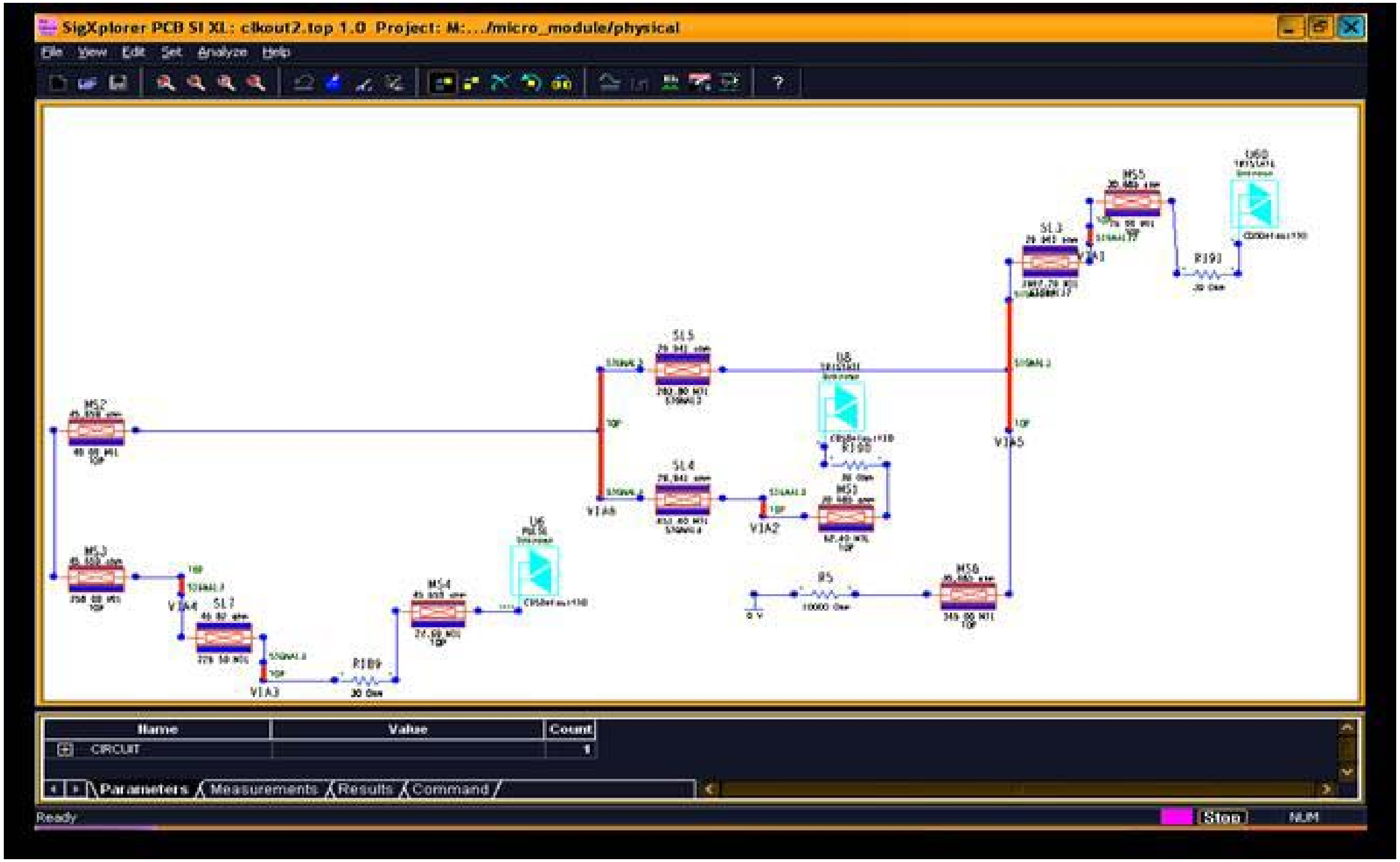


Proposed IEC 62014-3 core switching noise coupling model

Slide courtesy of Etienne Sicard, INSA-Toulouse

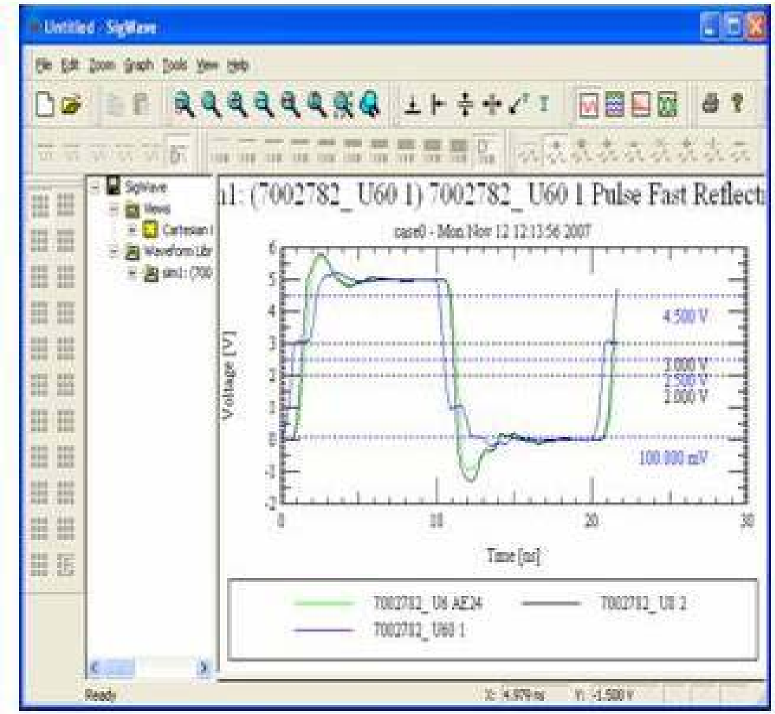
Signal Integrity and EMI-EMC

Test Net for SI and EMI

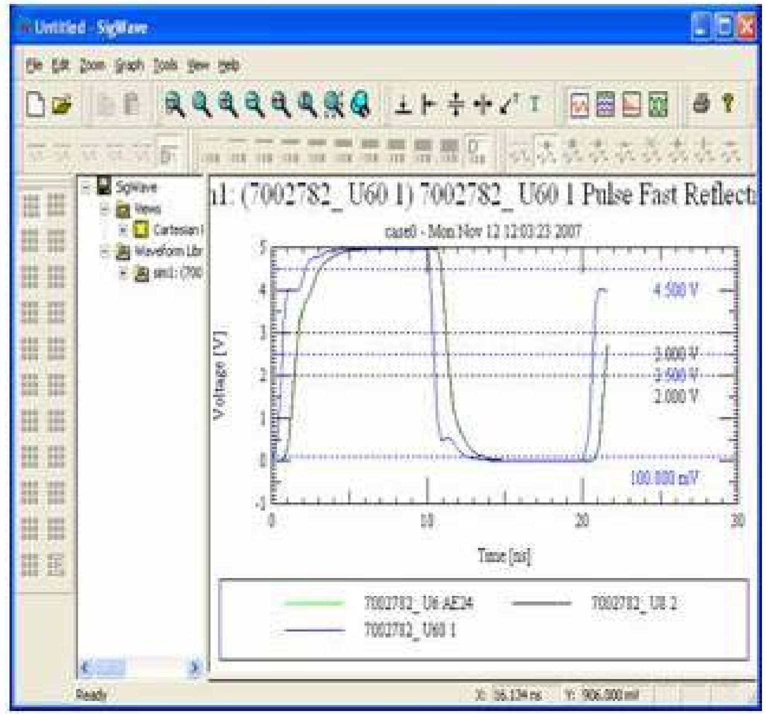


66MHz Clock Topology as Modified

How SI is Affected by Overshoot



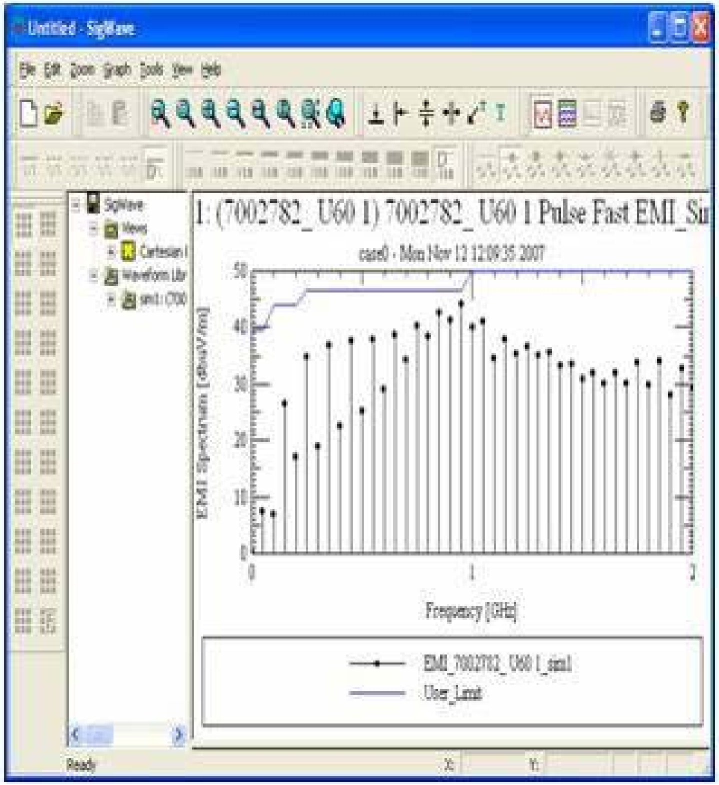
Before Termination



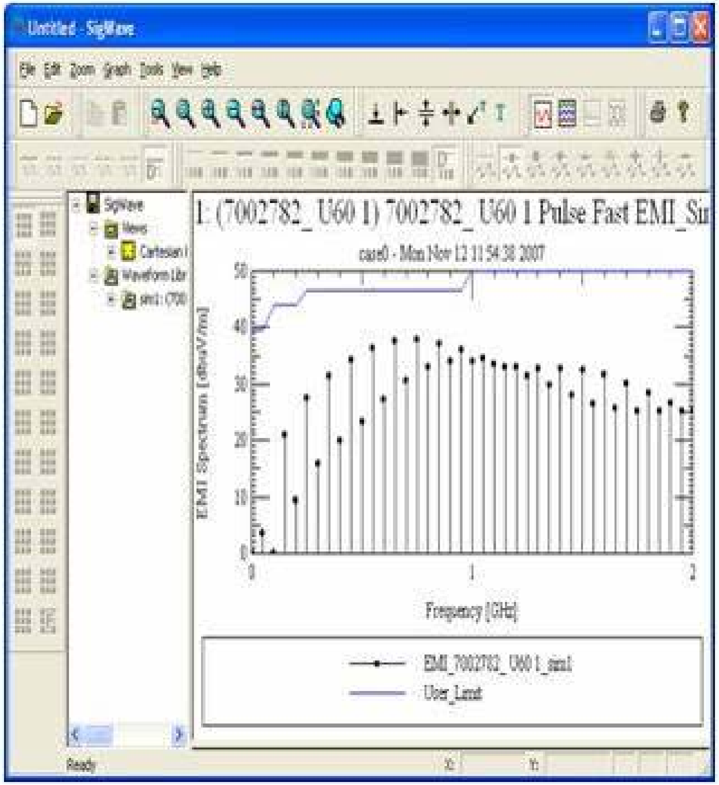
After Termination

Before termination, SI and stress on the receiver is not a high concern – the real payoff will be in EMI control as shown in the next slide.

How EMI is Affected by Overshoot



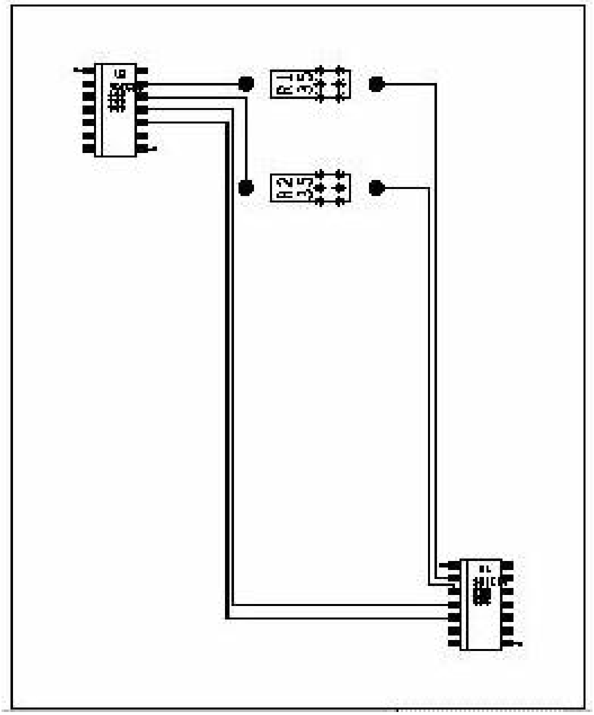
Before Termination



After Termination

The SI Engineer has to manage harmonics out to about the 5th .
The EMI engineer has to manage harmonics out to, perhaps, the 100th.

Example of Virtual Test Board



The board on the left has the following stackup:

top: 1.2 mil Cu signal Zo = 89Ω
next: 12 mil FR4 (εr = 4.5)
next: 1.2 mil Cu shield Vcc
next: 12 mil FR4
next: 1.2 mil Cu shield GND
next: 12 mil FR4
bottom: 1.2 mil Cu signal Zo = 89Ω

Etch width is nominally 6 mils

For the shielded version outer shield layers of 1.2 mil Cu spaced by 12 mils of FR4 were added

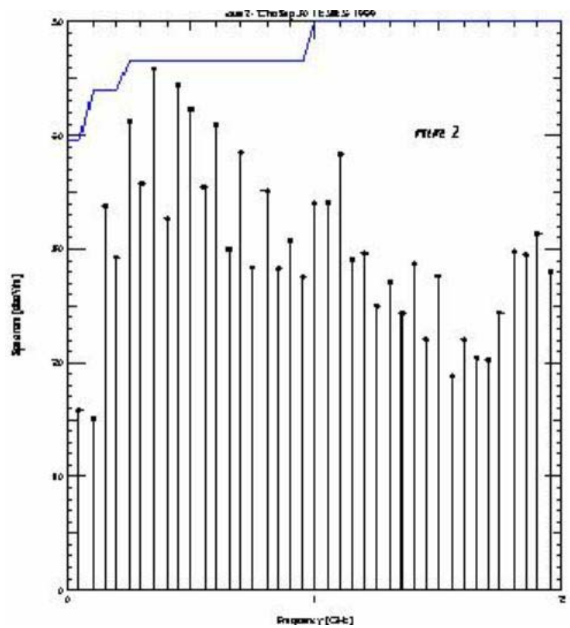
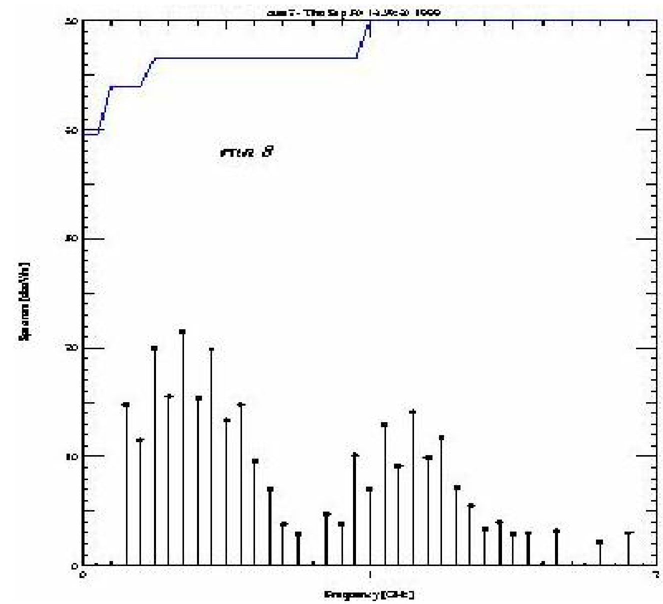
The nominal 6 mil etch on such an inner layer results in Zo = 59.6 Ω

The board is about 3 inches long.

Layout of the Test Board

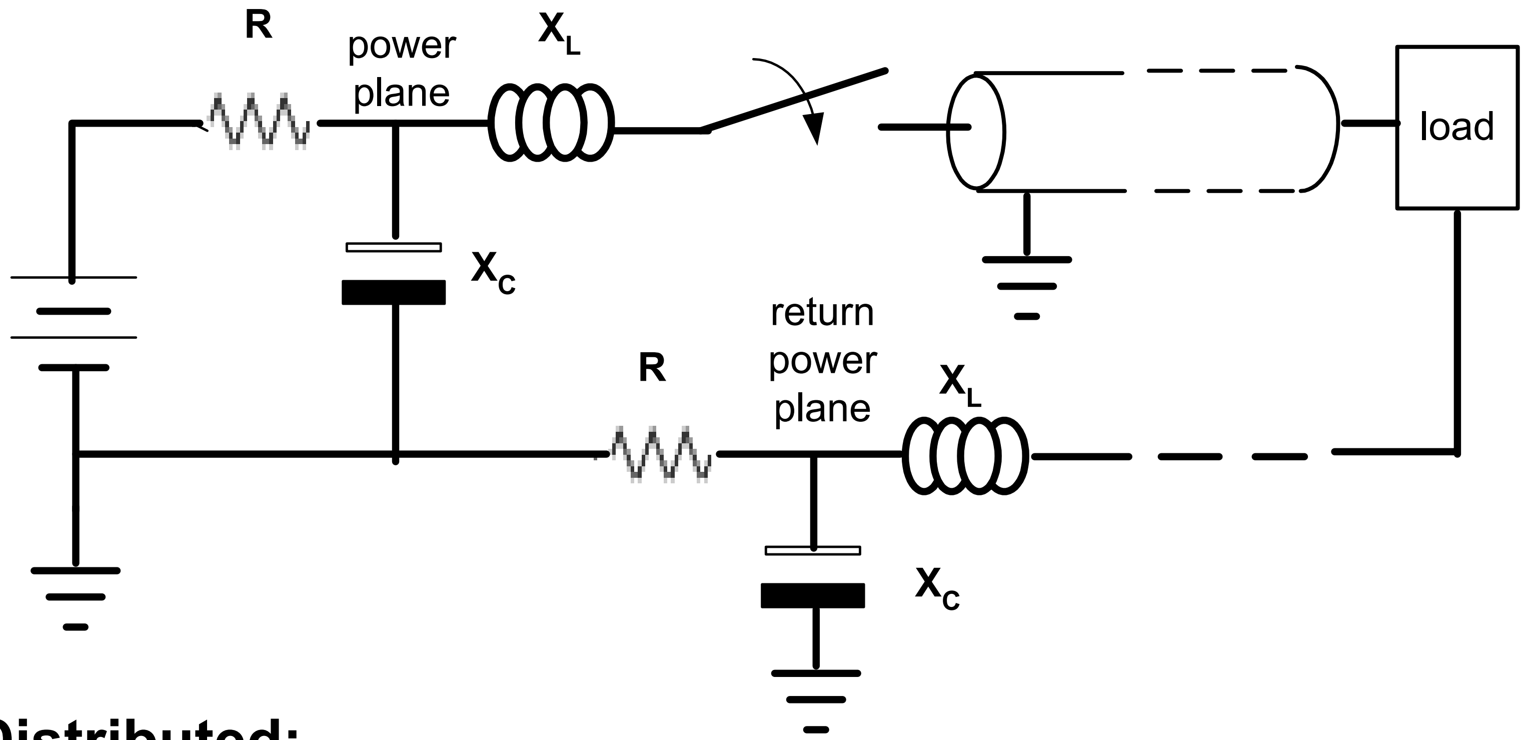
Stackup of the Test Board

Virtual Test Board
Before and After EMI Treatment

	
Unshielded, Unterminated, Non-Constant Impedance Net	**Shielded, Terminated, Constant Impedance Net**

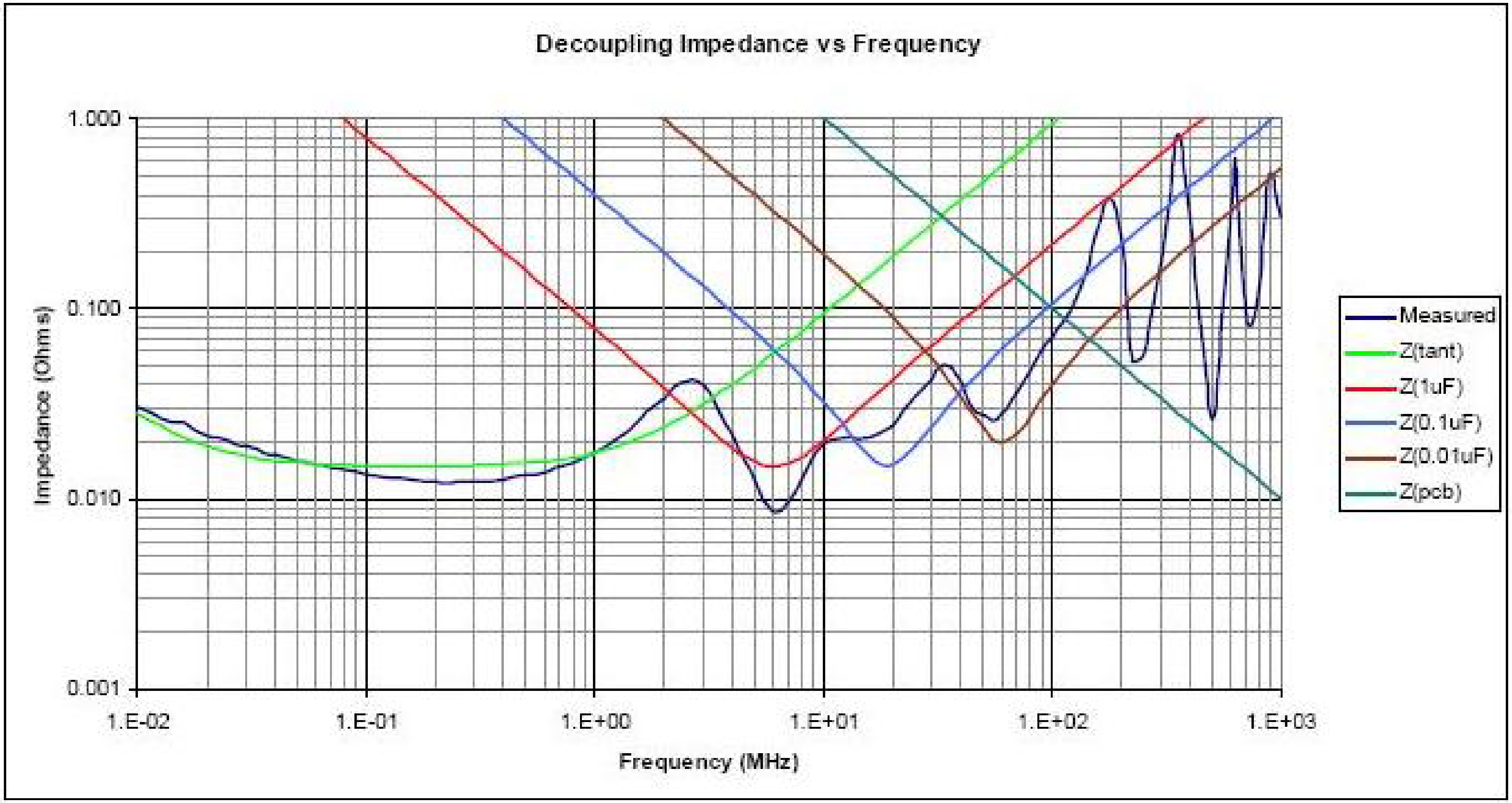
Power Integrity (PI) and EMI-EMC

Power Bounce (& Ground) Basics



- **Distributed:**
  $v_R = iR$, $v_C = iX_C$, $v_L = iX_L$, $X_C = -j/2\pi fC$, $X_L = j2\pi fL$
- **Switch characteristics: V-I & V-T curves, pin parasitics, etc. See the IBIS Model.**

Bypassing the Power Supply for PI



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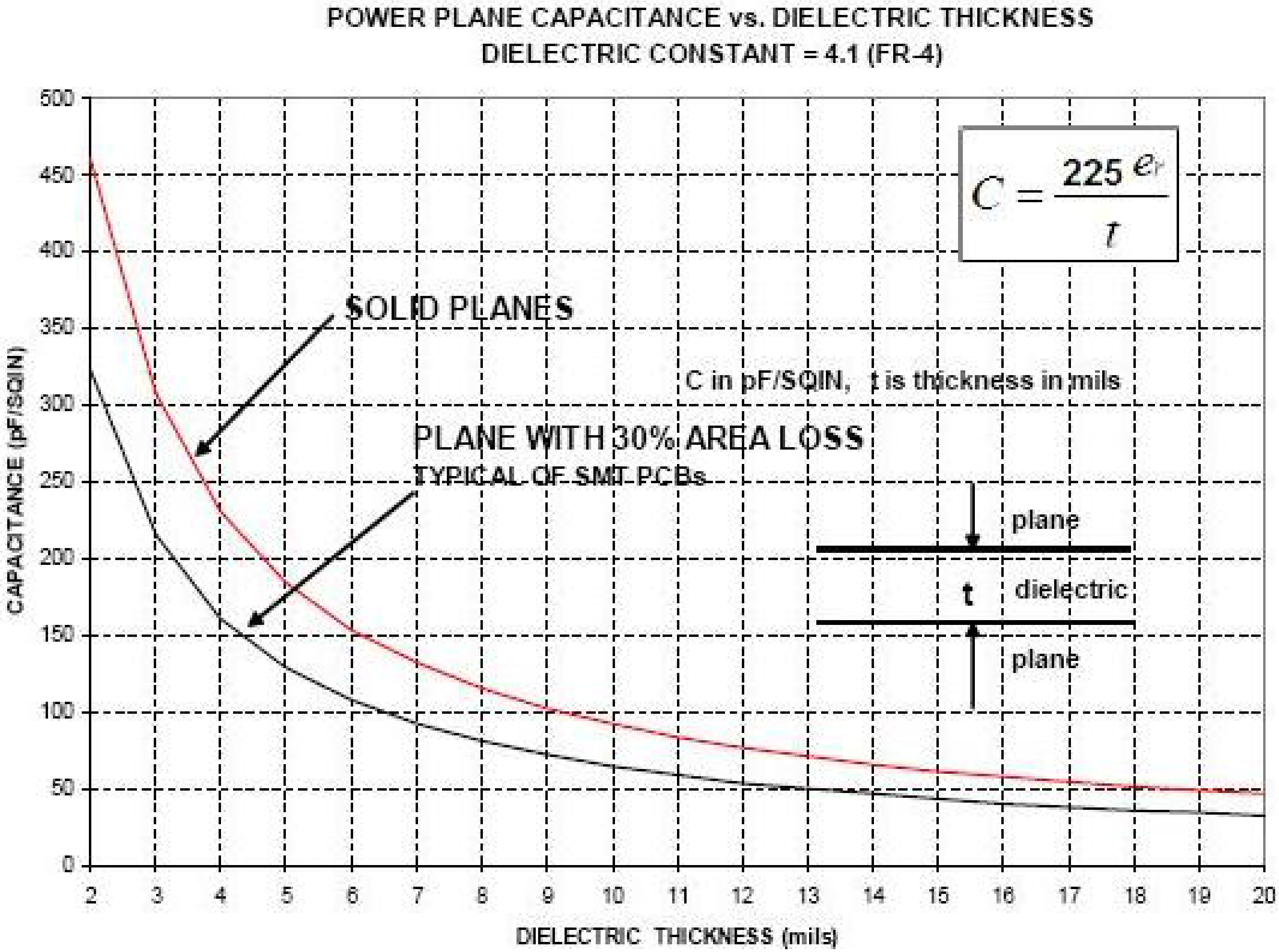
Interplane Capacitance



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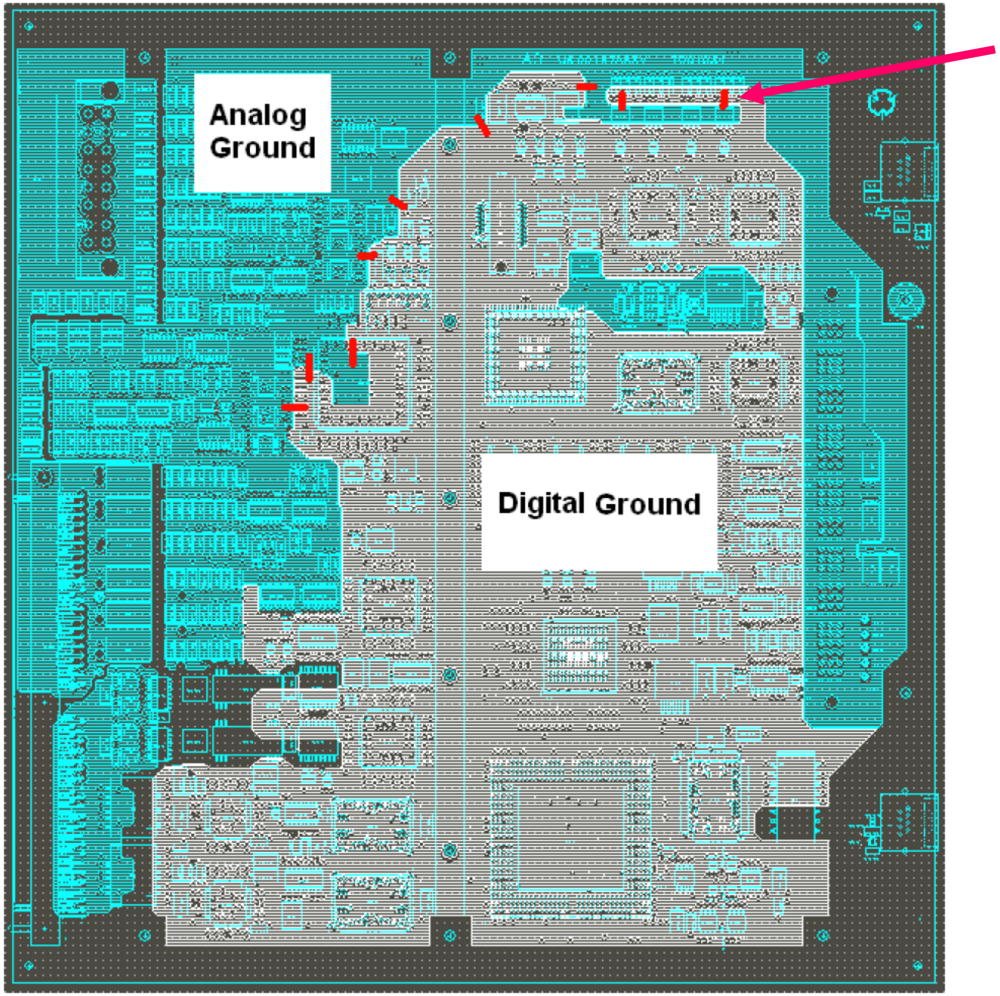
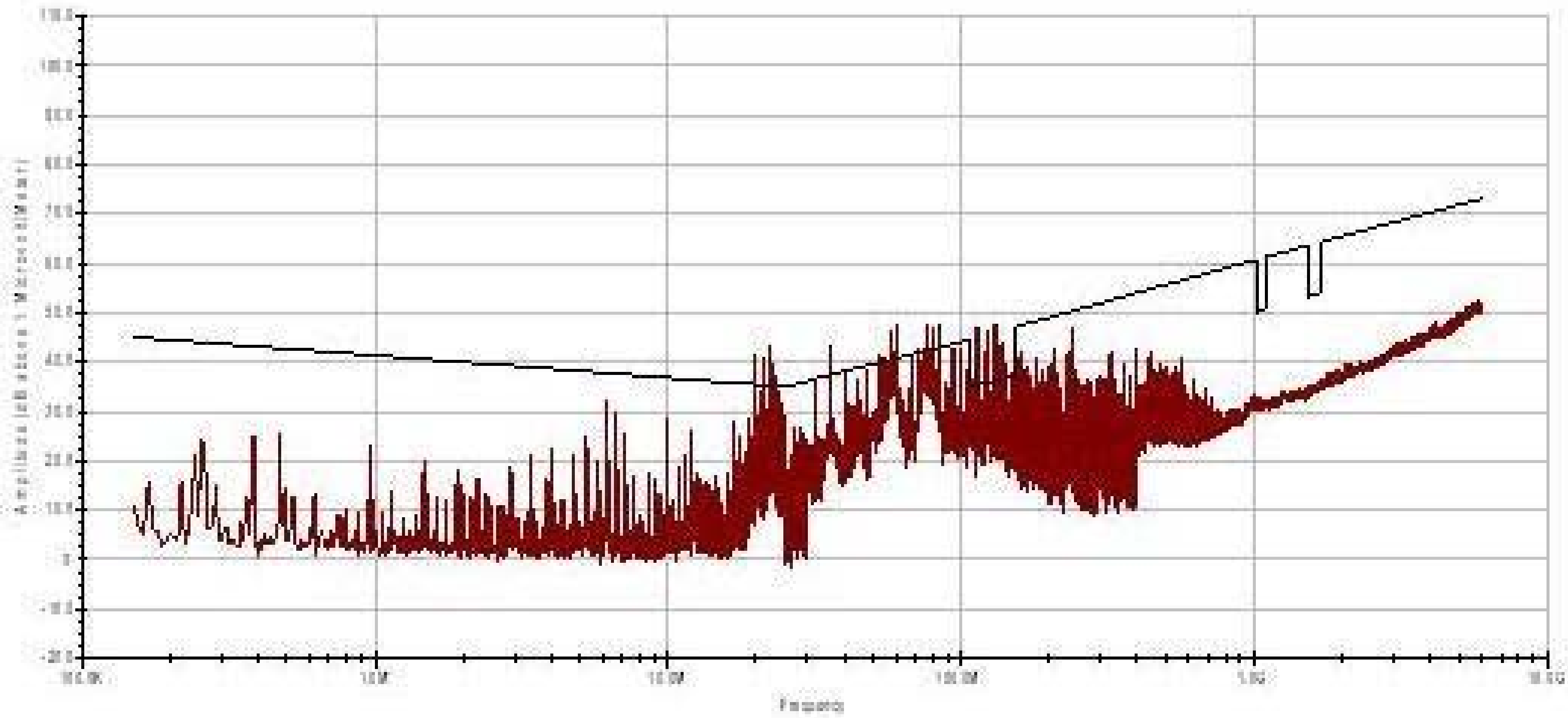
Splitting Ground Planes: An Example



- Analog ground plane and digital ground plane were "stitched" together at 9 locations on this PCB
- This change was done to improve both radiated emissions and susceptibility (300 – 400 MHz)

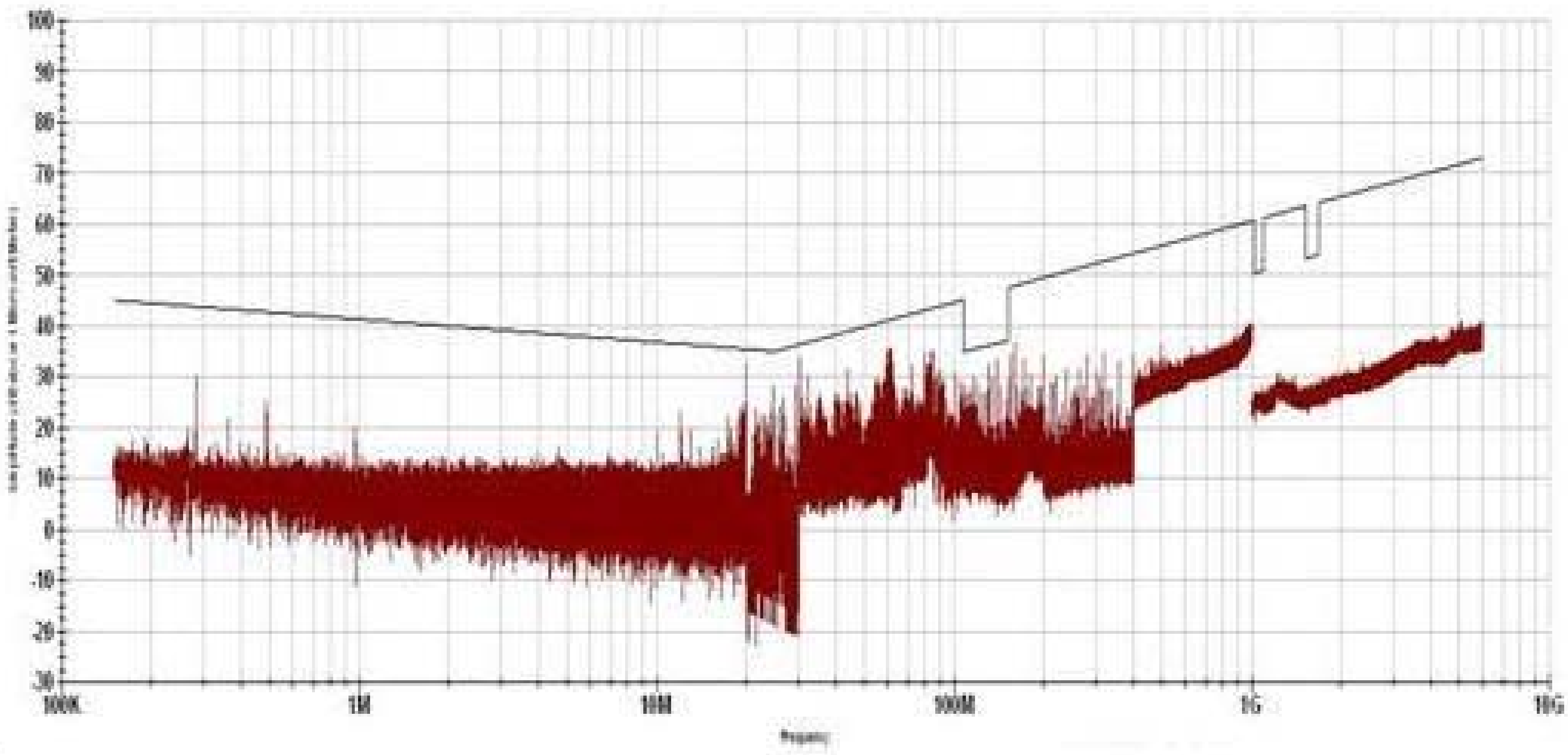
Before Stitching

Radiated Emissions

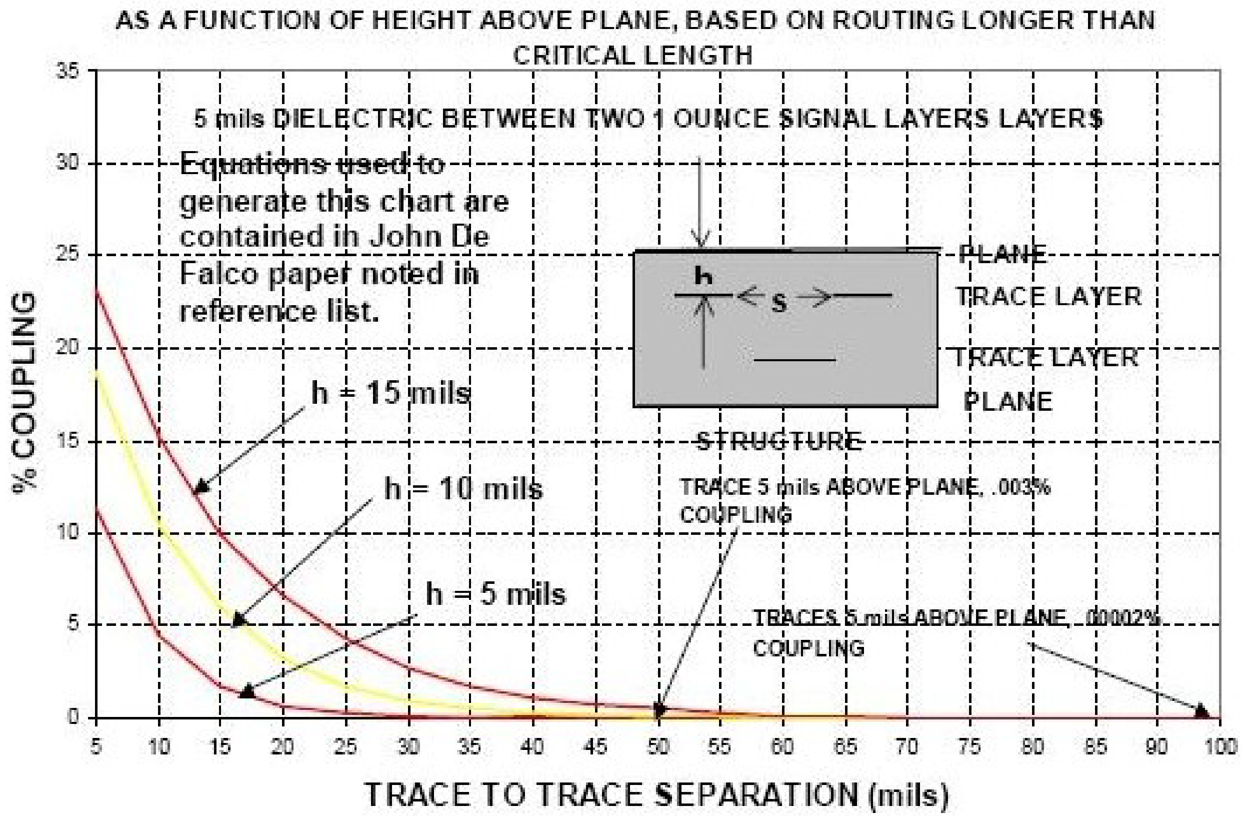


After Stitching

Radiated Emissions



Stripline Crosstalk



- **Slide courtesy of Lee Ritchey, Speeding Edge. Used with permission.**

Observations About Crosstalk

- **Above audio (10kHz) electromagnetic energy stays very close to a wire it is flowing on when its reference plane is close.**

- **Electromagnetic near field coupling strength falls off at about 1/(distance)^3. At 10 mils away from a trace 5 mils from a reference plane less than 5% crosstalk coupling is detectable.**

- **Split planes, rows of ground vias around a PCB perimeter, guard traces, and edge plating to control crosstalk coupling and EMI should be closely critiqued when frequencies are above audio.**

Board Level EMI-EMC

Visualization Using Computational Electromagnetics Tools

Near Field EMI Simulators

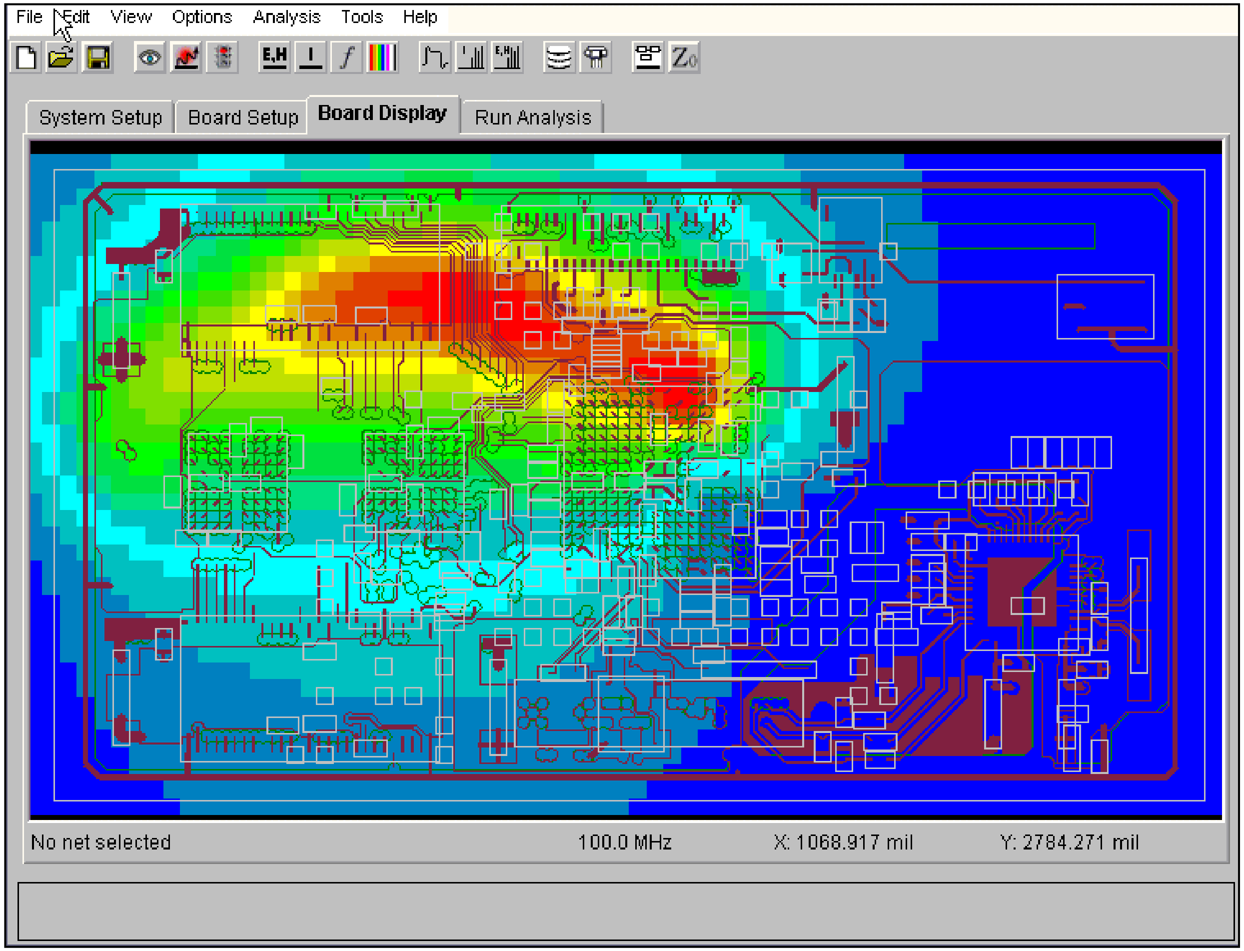


Image Courtesy of Johnson Controls Automotive, Inc. Used with permission

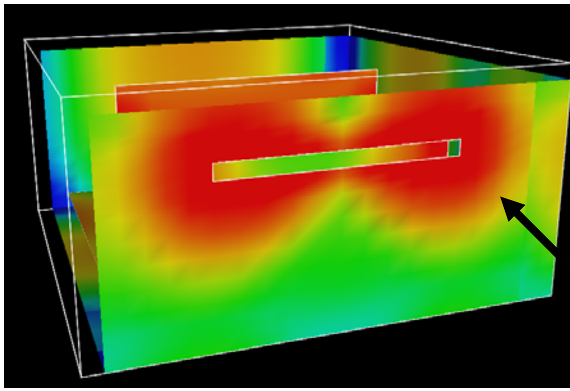
- **A compact model (E-H vectors, etc.) is extracted for use in CEM tools at the next level up amongst all mainstream EDA vendors**
- **See also: EMScan**

Line Replaceable Module Level EMI-EMC

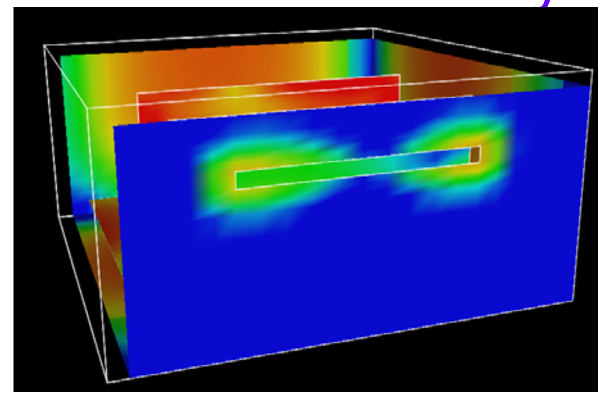
Computation and Visualization with CEM Tools

3D Full-Wave EMI Simulators

Baseline

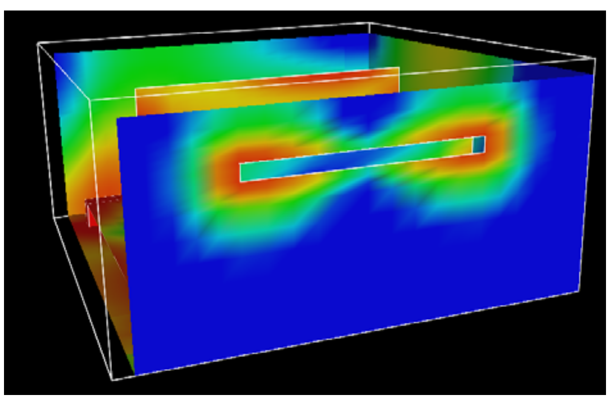


Ground Pins Only

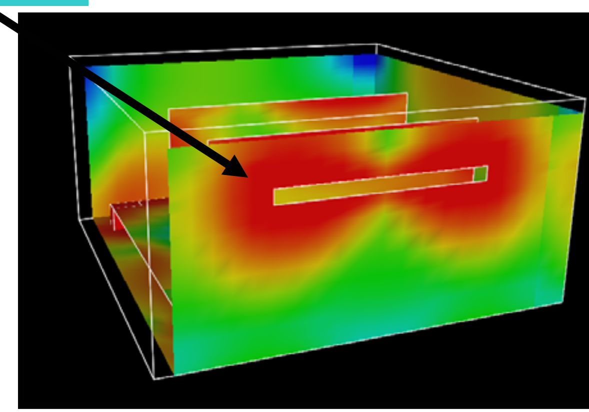


Strong Coupling to Slot-WHY?

Standoffs Only

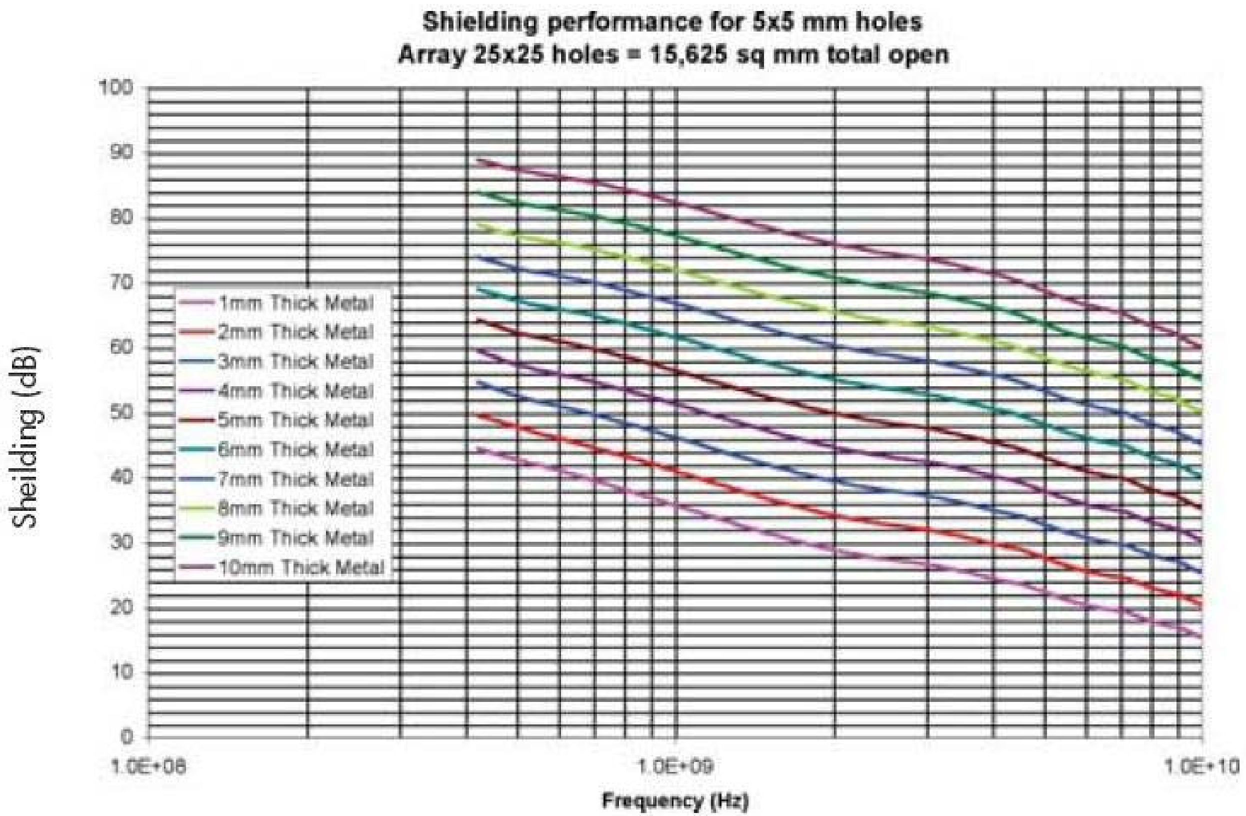


Pins and Standoffs



Slide courtesy of FloEMC/CST and David Johns. Used with permission

Example: Non-CEM Tools: Shielding Effectiveness of Holes

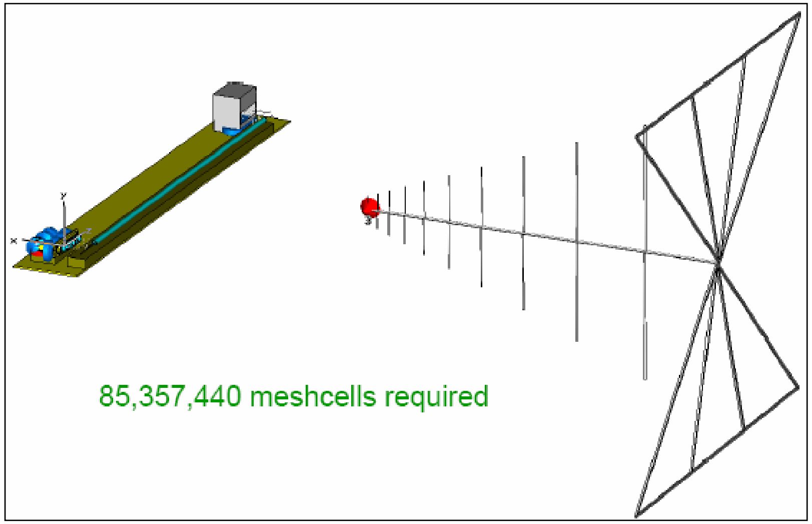


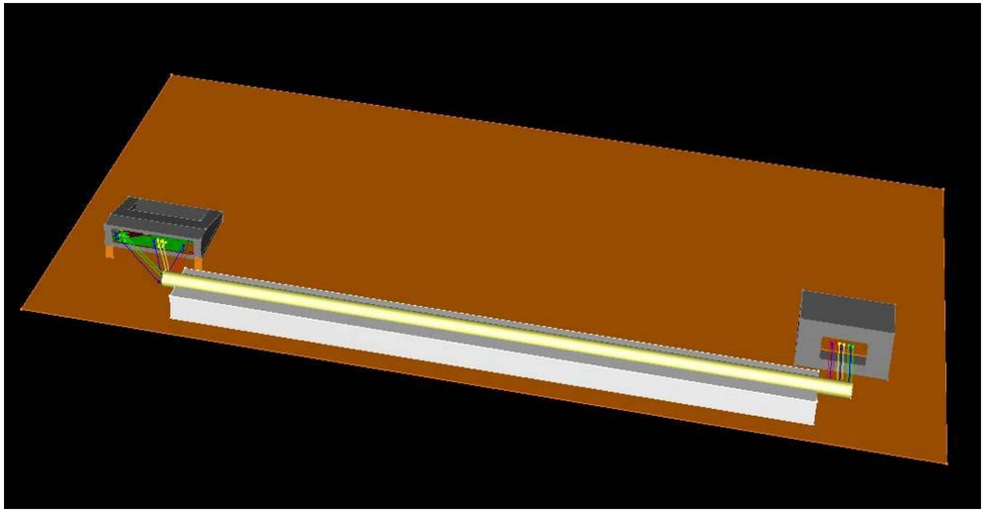
Slide courtesy of IEEE and Bruce Archambeault. Used with permission

System/Sub-System Level EMI-EMC

Visualizing the Test Chamber with CEM Tools

The Virtual Test Bench





Slide courtesy of CST/FloEMC.
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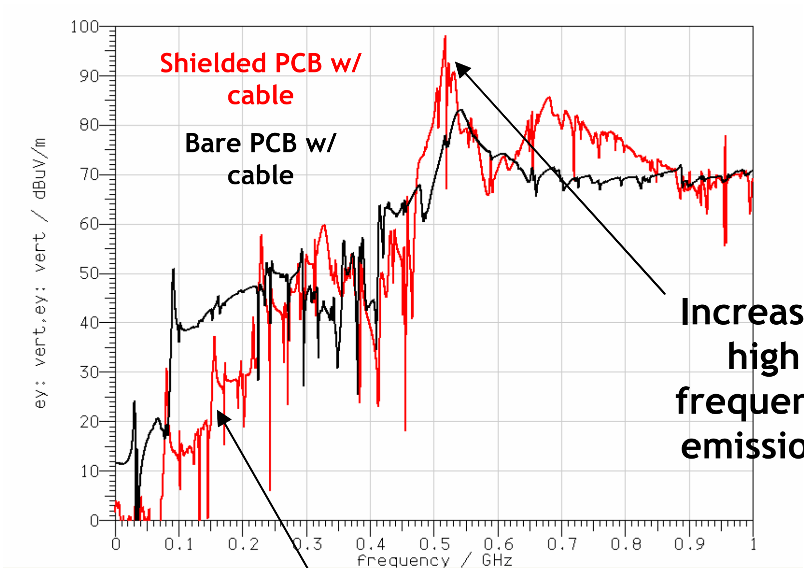
Simulation vs. Measured

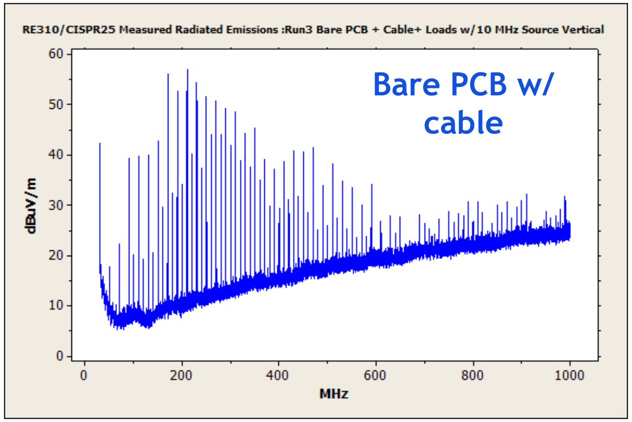
Bare PCB w/ cable vs. Shielded PCB w/ cable

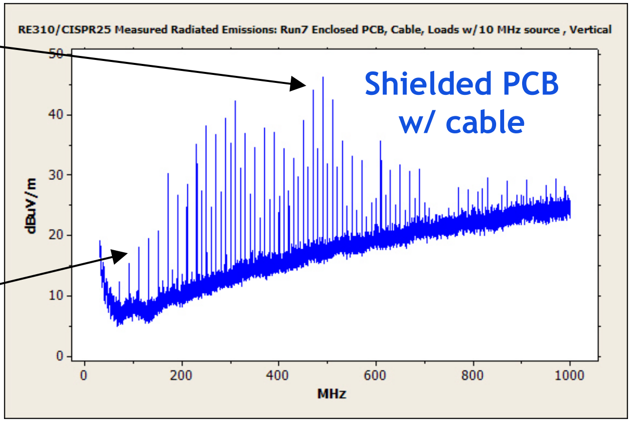
Simulated emissions (broadband source)



Increased high frequency emissions

Reduced low frequency emissions





Measured emissions (30 MHz CLK)

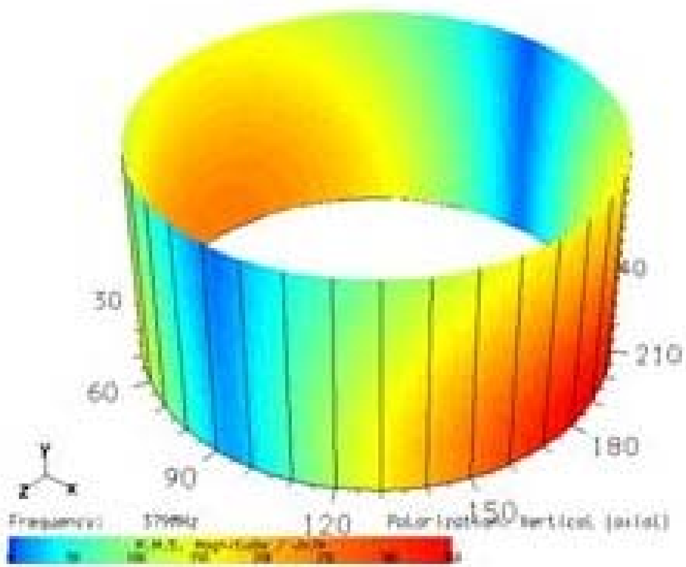
CST

Slide courtesy of CST of America. Used with permission.
Presented at IEEE EMC 2008 Symposium

Far-Field EMI Simulators

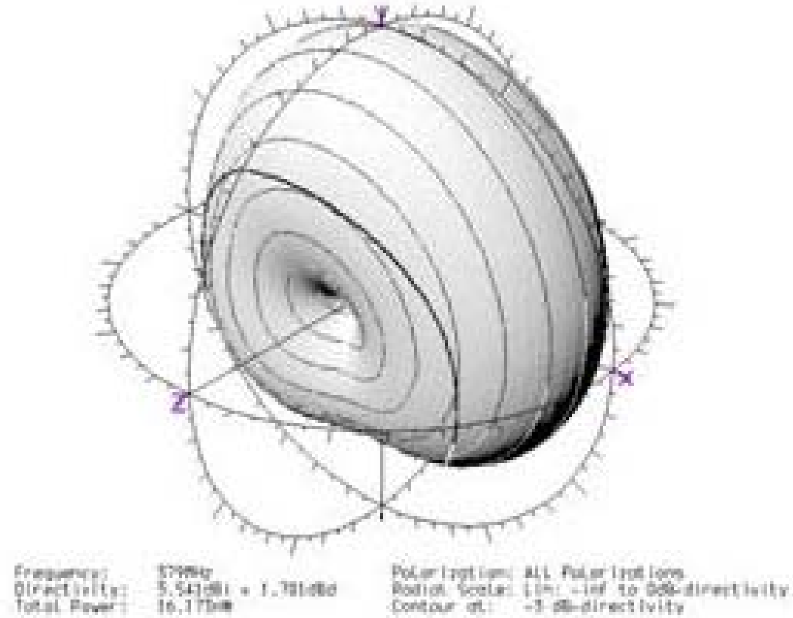
Simulators of this type help the visualization of issues raised in the previous slide

U1 Star com Box



3m cylinder scan

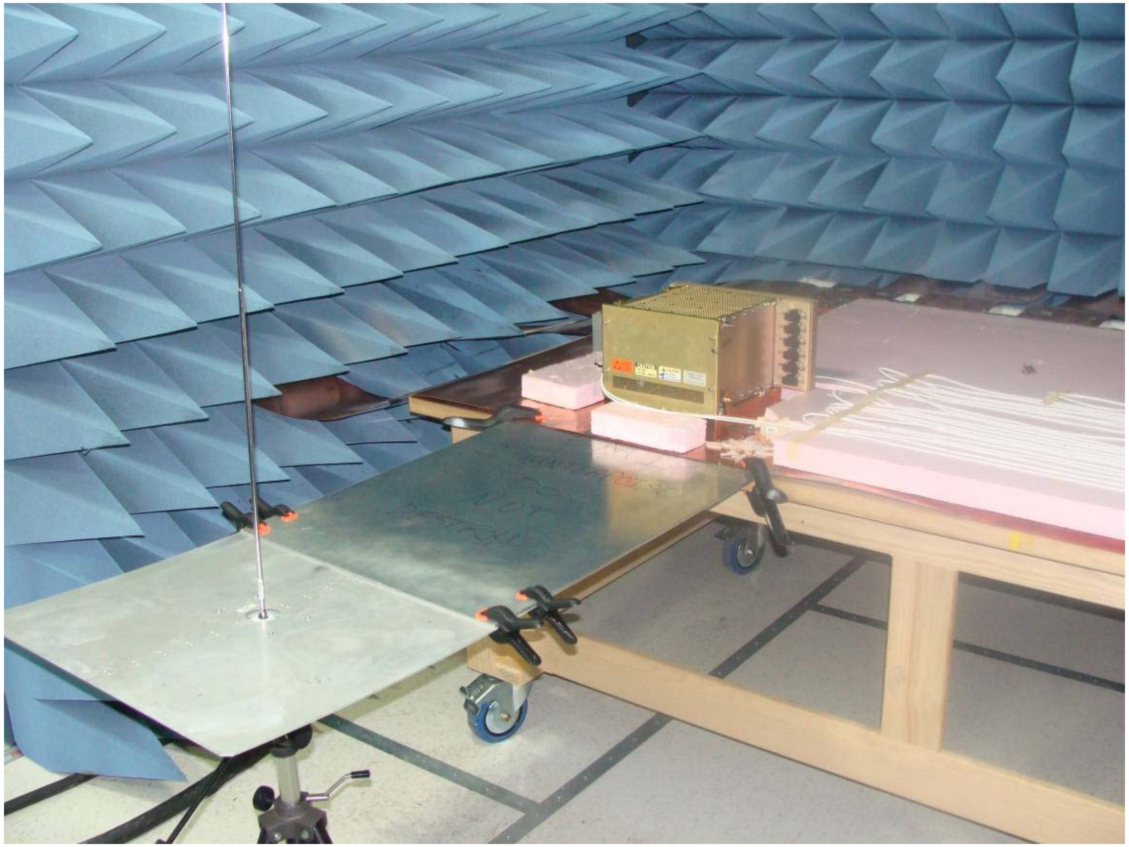
U1 Star com Box



Far-Field radiation

Slide courtesy of FloEMC/CST. Used with permission

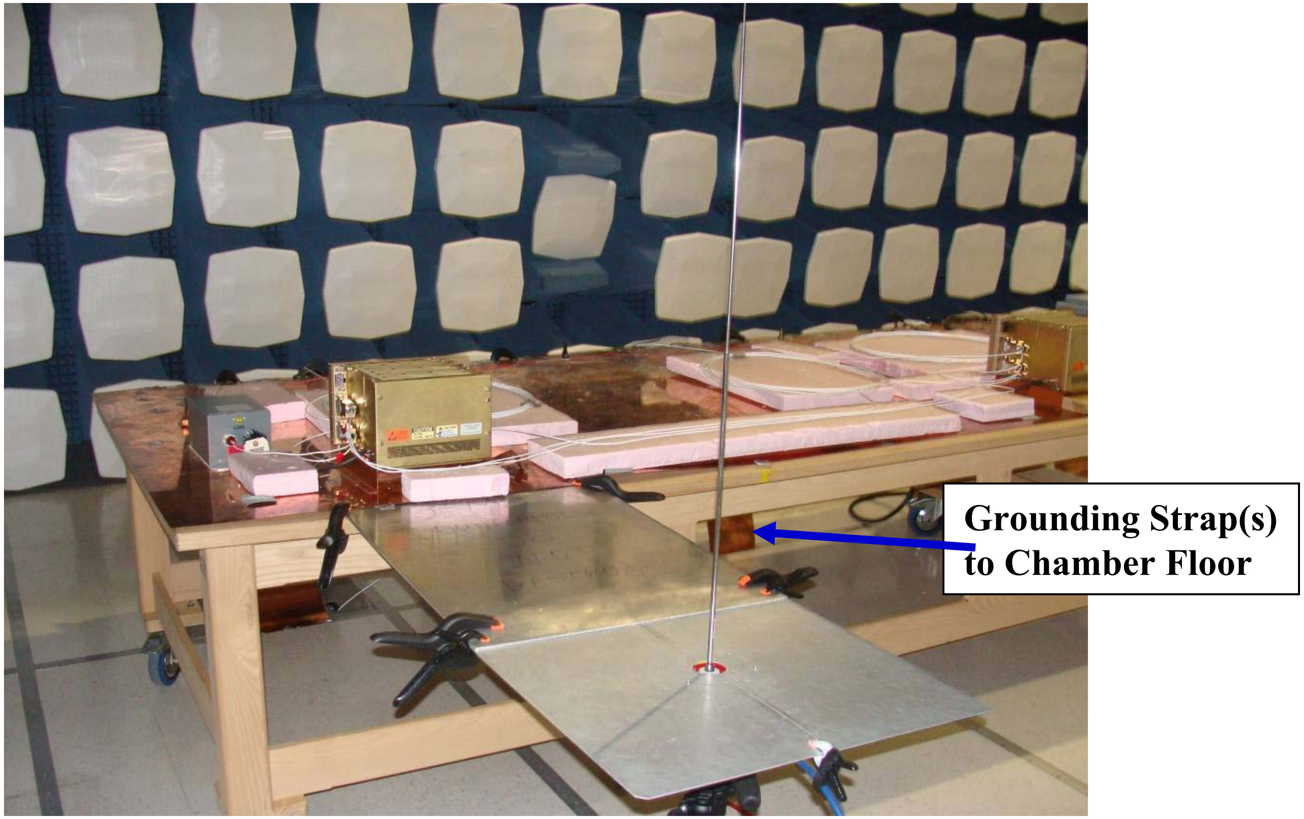
Active Rod Setup



The active rod monopole antenna, its counterpoise, the ground plane resonances, and the room resonances all interact

“Surprises” in EMI Test Chambers

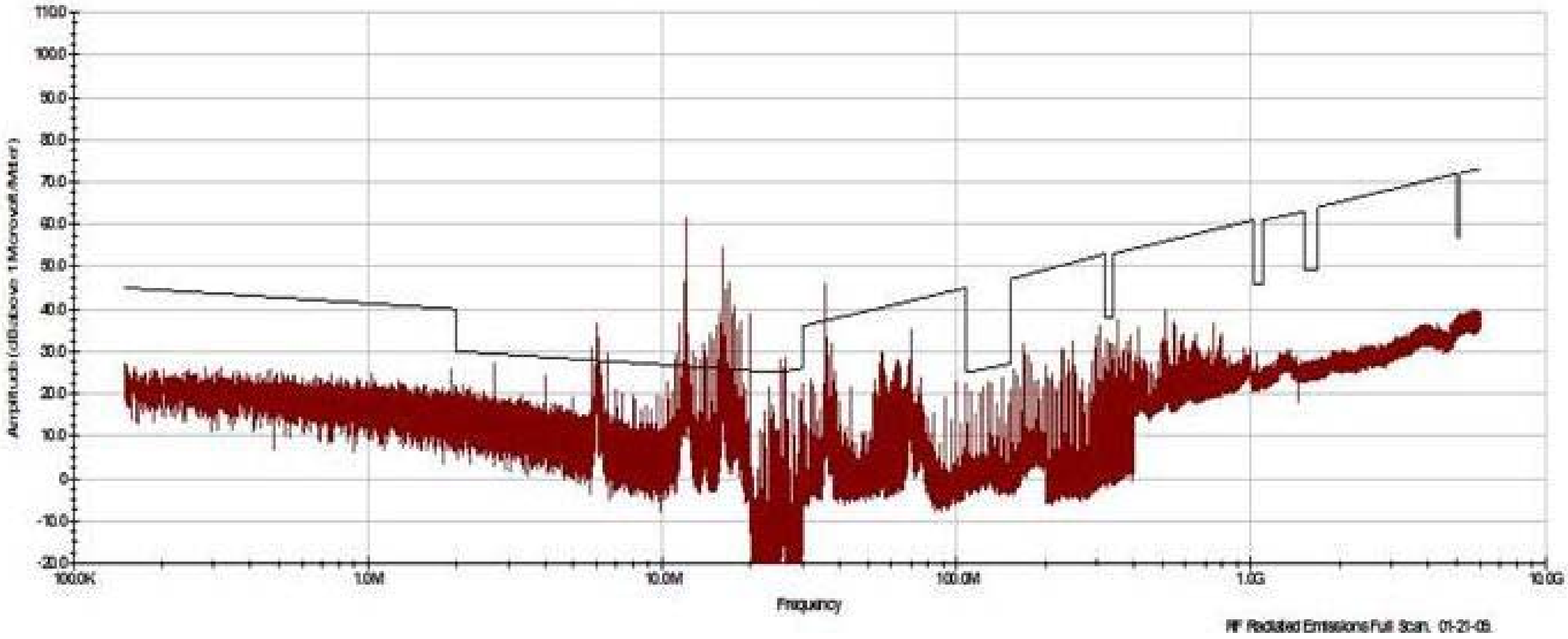
Experiment #1 in the 10 Meter Chamber



- **Setup near south wall in 10m chamber. Experiment to see if ferrite tiles are better than foam absorber cones.**

10 Meter Chamber South Wall Result

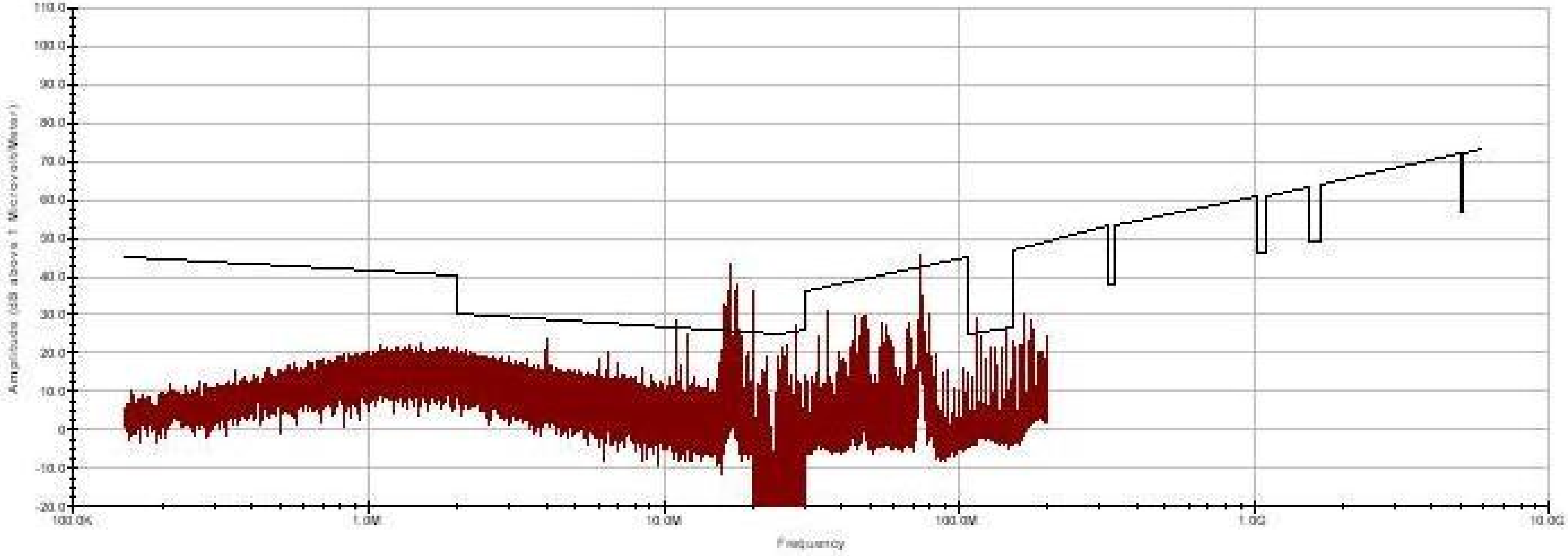
Radiated Emissions



- **Initially, HF band spurs are 25 dB worse than in MIL461 chamber!!!**

10 Meter Chamber East Wall Result

Radiated Emissions



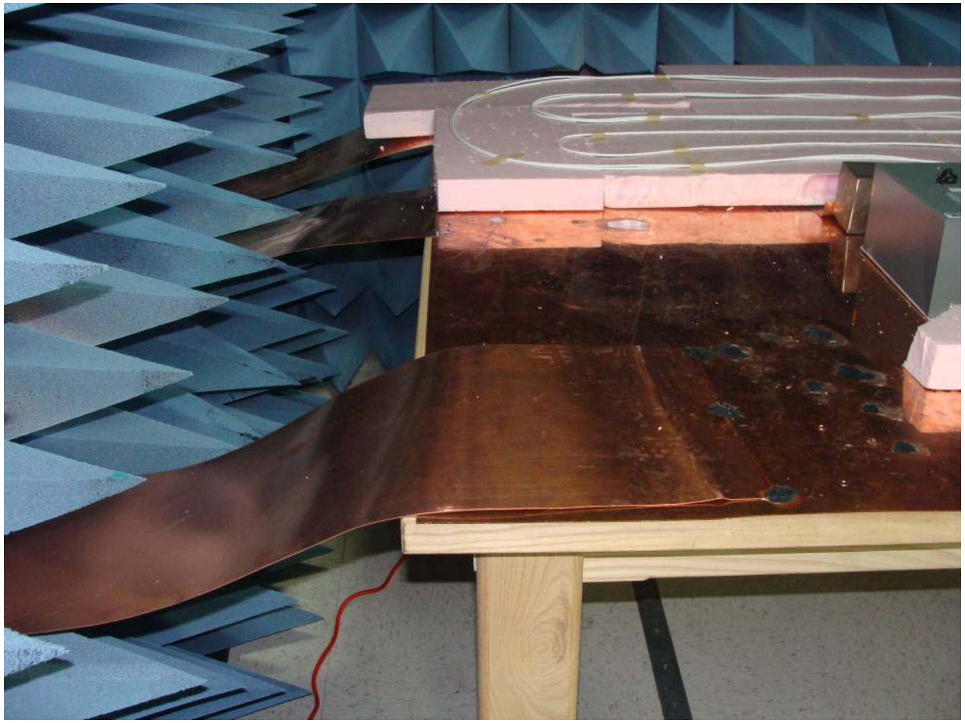
- **HF band spurs have immediately dropped 15 to 25 dB! Copper bench top still ground strapped to chamber floor.**

Model Suggested by Measurements

- Resonances and impedances of the PCB, Line Replaceable Module, test bench, grounding system, cables and test room all interact just the same as elements of a closed loop circuit interact

- Corollary: Separating out cause and effect in the test cell can be challenging

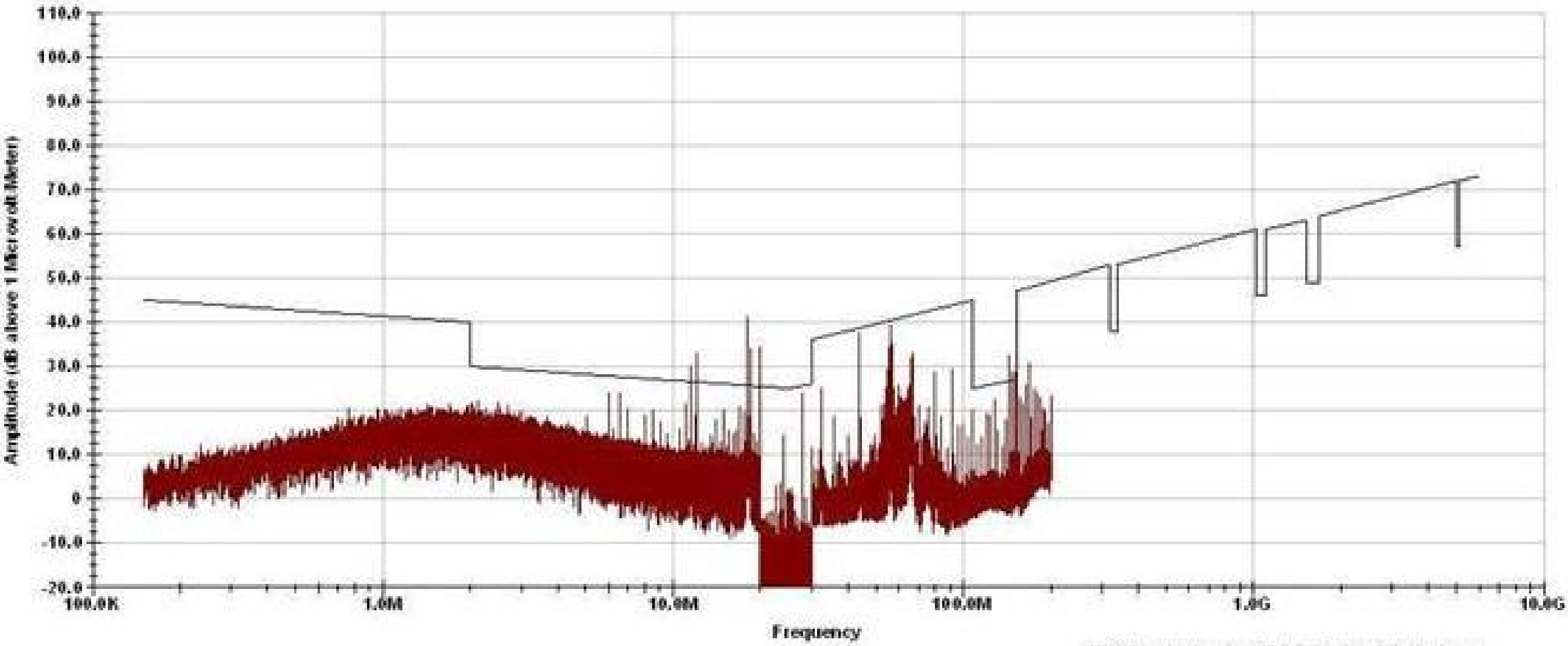
Experiment #2 Test Bench Grounding in MIL461 Chamber



- Test bench copper top is 2.5 x 7 meters
- Copper top ¼λ resonant near 15 MHz
- Corners are high impedance points
- Solution: ground corners to inner metal wall of chamber

Initial Results Without Corner Ground Straps

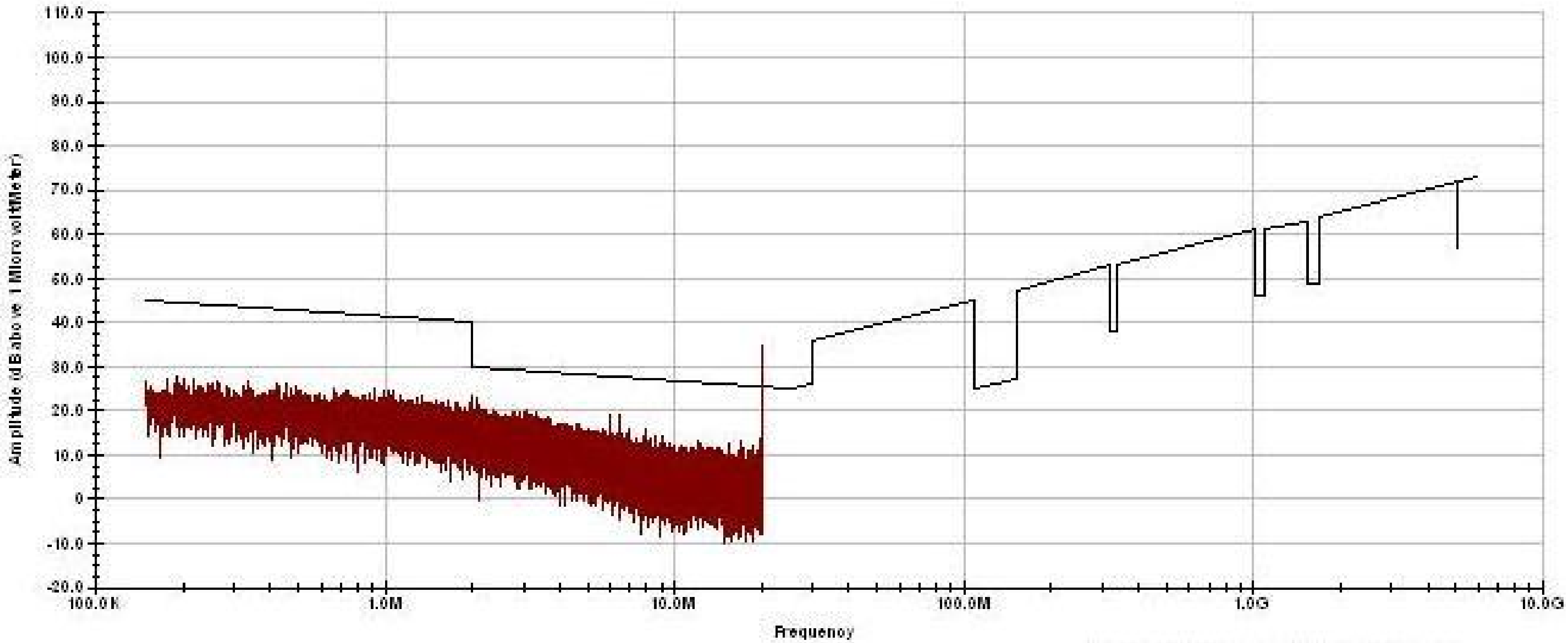
Radiated Emissions



- **Active Rod and BiCon: 150 kHz to 200 MHz**

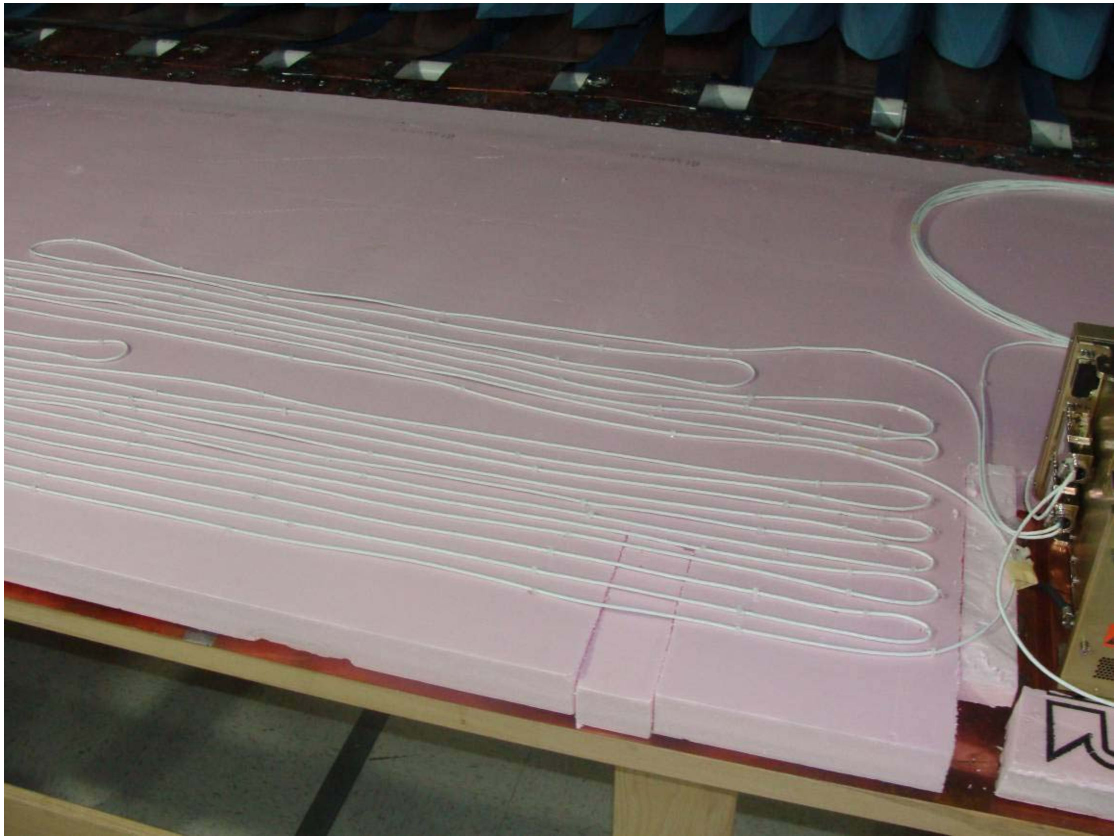
Grounding All Corners of the Test Bench

Radiated Emissions



- **Active Rod: 150 kHz to 20 MHz**

Experiment #3 Effect of Tight Cable Bends



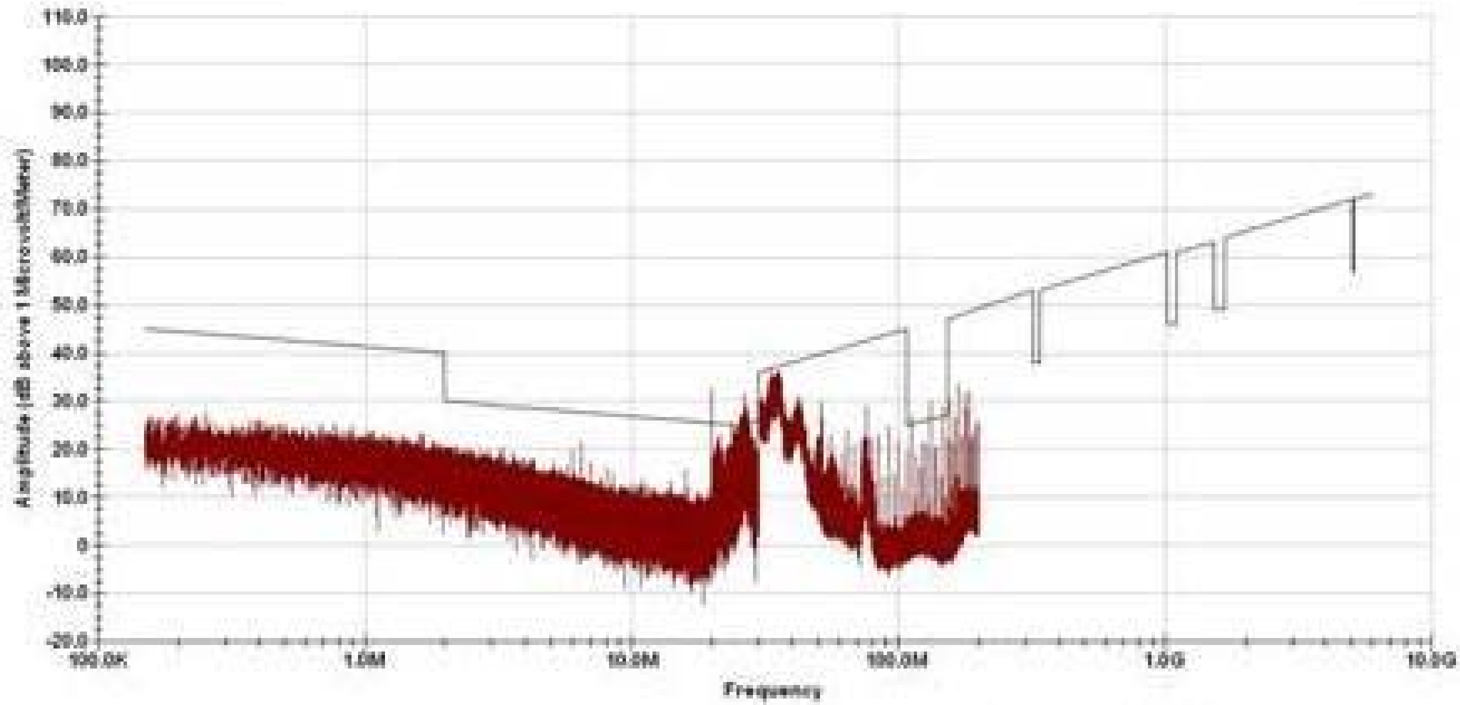
Tight cable bends stretch the braid apart on the outer part of the bend

Standard calling for "cable zigzagged on table" is MILSTD 461E paragraph 4.3.8.6.1

- **Here diameter of bends is approximately 1 to 1.5 cm**

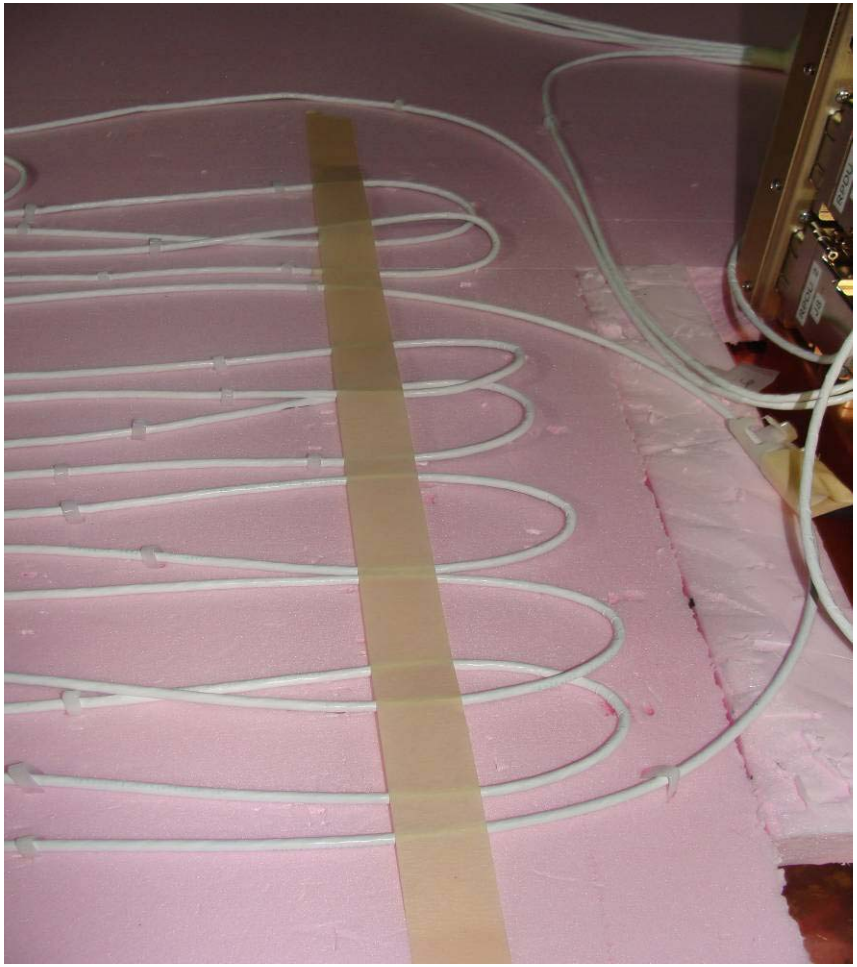
Tight Cable Bends: Result

Radiated Emissions



- **The high emissions from about 20 MHz to about 100 MHz did not exist before the TTP cables were bent**

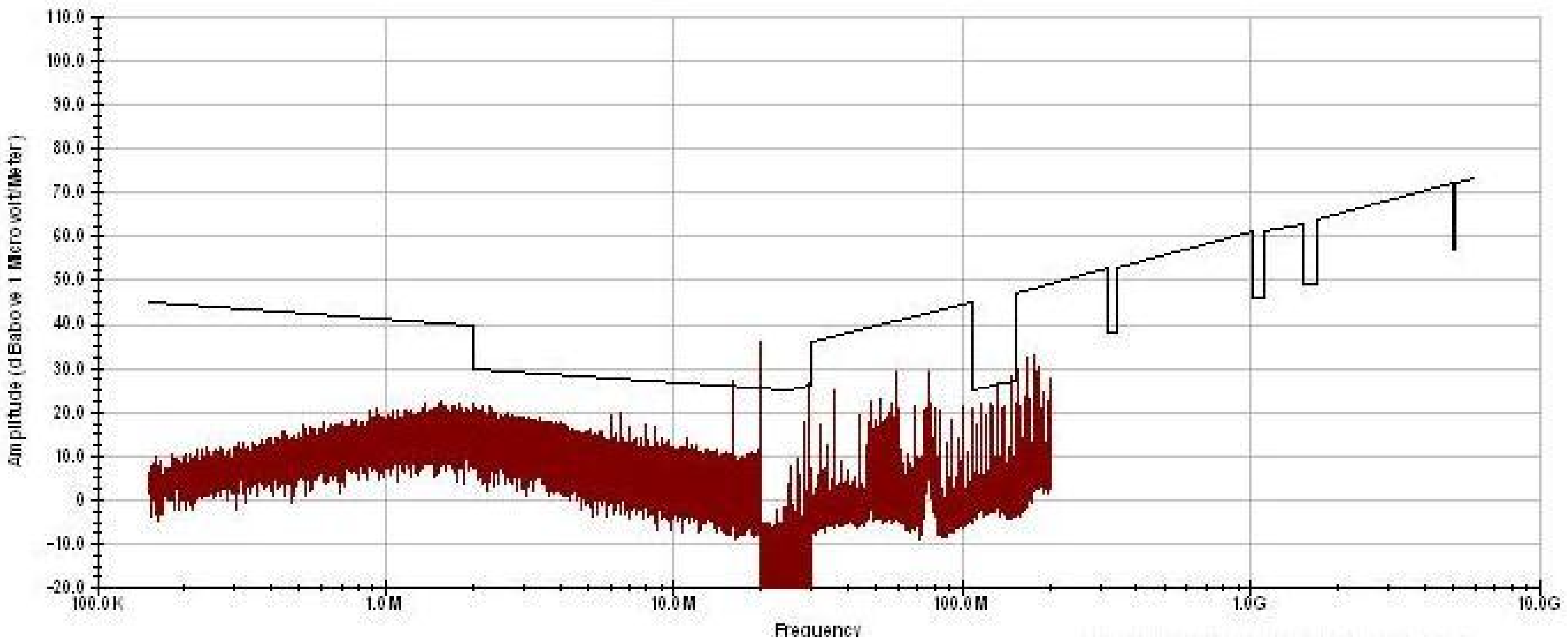
Gentle Cable Bends



- **Plastic u-shaped clips removed and cables allowed to assume a more relaxed bend**
- **Diameter of bends has “relaxed” to approximately 3 to 5 cm**

Gentle Cable Bends: Results

Radiated Emissions



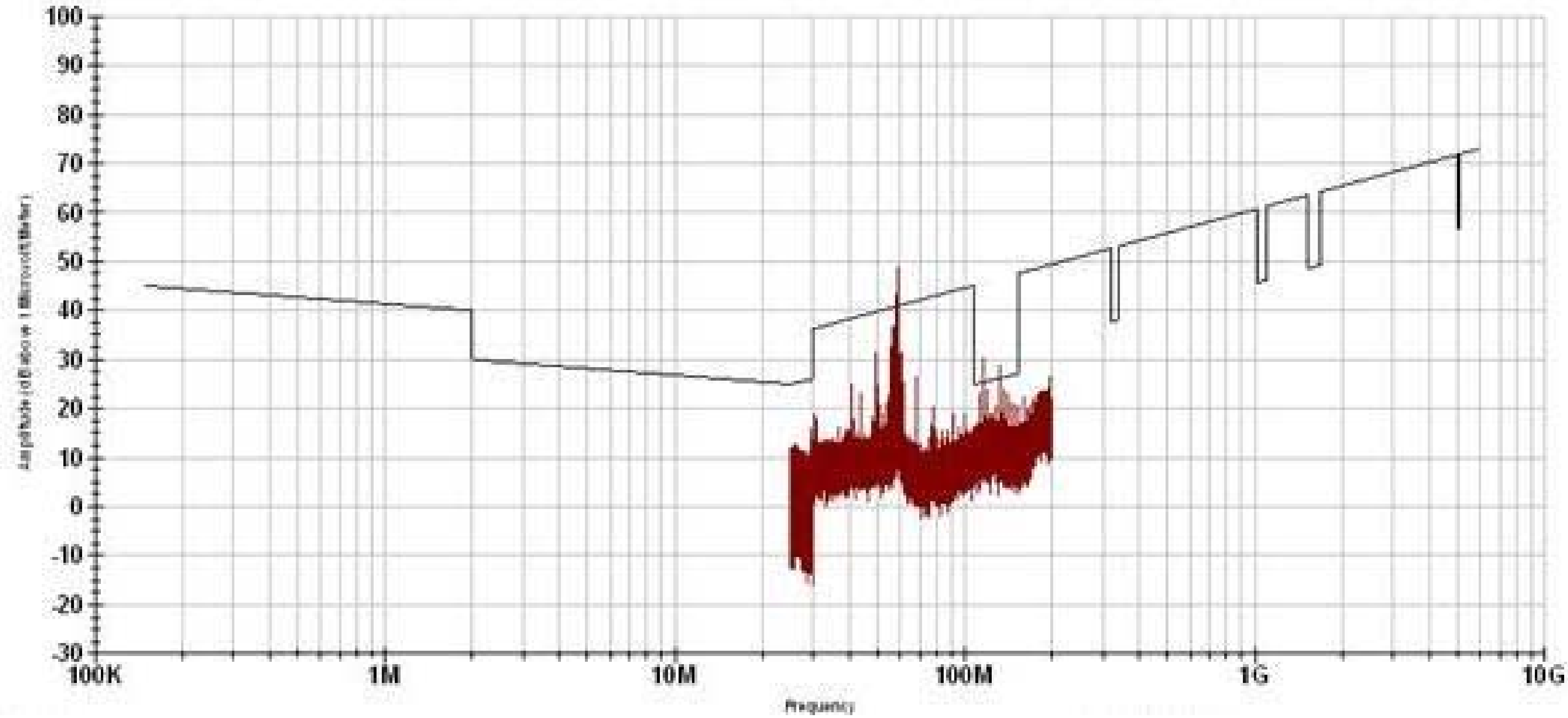
- **The high emissions from about 20 MHz to about 100 MHz have mostly disappeared**

Message

- Hindsight translated into foresight reveals that the results of EMI-EMC Regulatory Testing are predictable. Therefore, they are:
  - Controllable by design and design choice
  - Can be planned for
  - The responsibility of the product designer
  - NOT black magic
- Simple observation indicates that $100 spent wisely at the start of a project can easily save $100,000 in Test-And-Fix
  - Test cell rental, personnel, and engineers can easily burn more than $7000/day
  - However, the real savings of “Right the First Time” are in shorter development times, less frustration and waste

Pigtails 101

Radiated Emissions



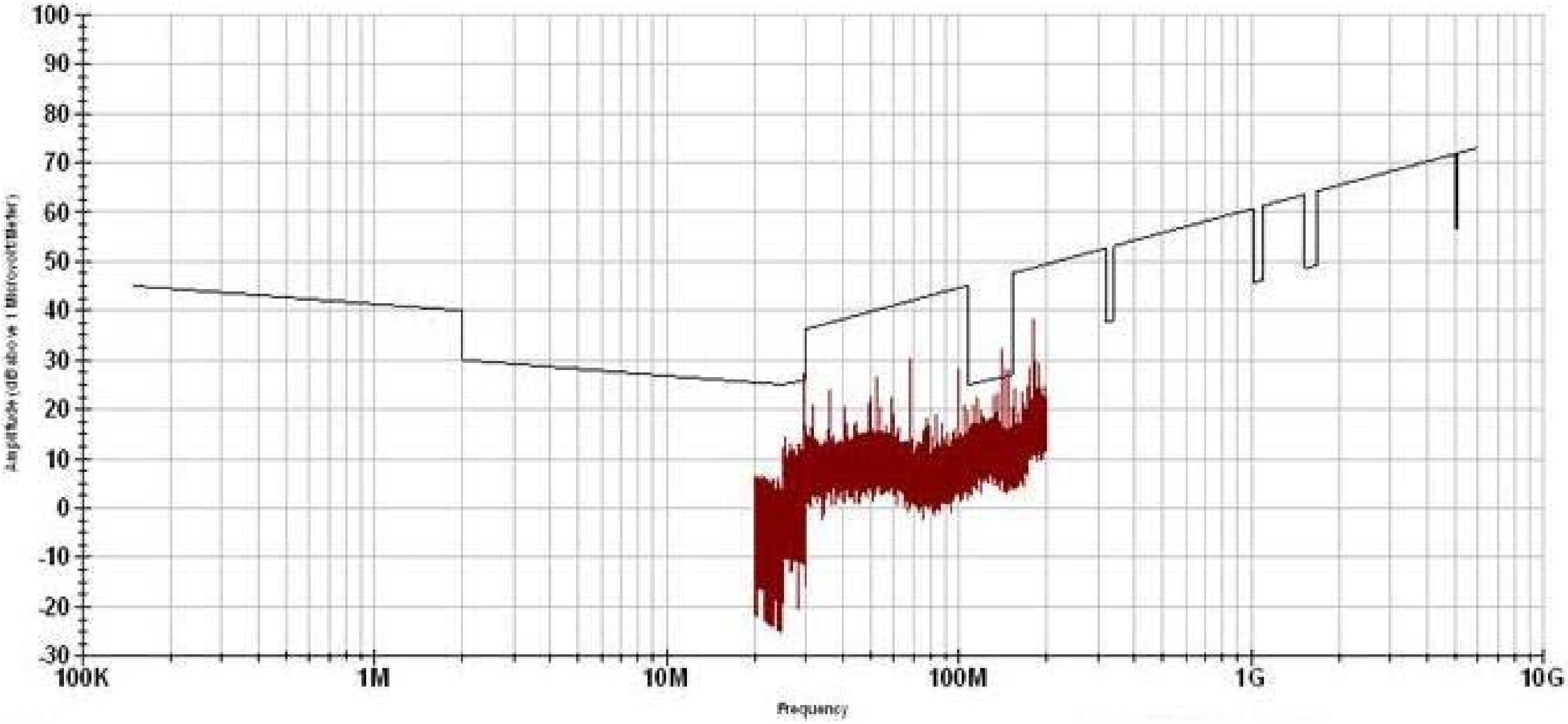
- **Exposed pigtail is 4 cm long at bench end and 6 cm long at connector end. Shielded return wire is 5 m long.**

A 5 m = Lambda Antenna has a Frequency of 59.958 MHz

- Inductive impedance of 4cm of ground lead at 60 MHz is about 360 ohms. This is close to the open circuit impedance to free space of 377 ohms.
- Both the 28 VDC return wire and its shield are then copper tape shorted to the bench at that termination

Death to Pigtails!

Radiated Emissions



- **Results of copper tape short to bench of of 5 m shielded return**

Instrumentation Illusions*

- During test and debug in the partial anechoic chamber at times the RFI spectrum measurements didn’t make any sense when a fix was tried
- When we looked real-time we saw spur levels modulating up and down by 7 to 9 dB!
- Two noise frequencies, 800 Hz and 4 MHz, were beat-frequency modulating with each other
- Depending on spectrum analyzer settings and intermodulation phases along the noise signal the detected level would vary by 7 to 9 dB!
- *More consistent measurement results were obtained with an averaging spectrum analyzer measurement
- The two noise frequencies provide clues as to where to look to implement noise lessening improvements

Summary

- **EMI**
  - Is driven by the strength and speed of the circuit drivers
  - Is driven by the discontinuities and resonances of the transmission path
  - Extends to much higher harmonics than SI issues

- **Technology has evolved**
  - Early TTL (ca.1960s) had a t_r of 30 ns and a V_{th} of a couple of volts - Designers sometimes used split return planes and pigtails
  - Today's CMOS uP cores typically have a t_r of 0.25 ns and a V_{th} of .35 volts
  - Soon we can expect to see I/Os with a $t_r < 0.1$ ns and a V_{th} of .35 volts

- **Planning for "Right the First Time" EMI performance requires an integration of the knowledge of how a PCB will be used at the system level and how it will be configured and tested to pass Regulatory requirements**

Summary

- EMI can be controlled by sophisticated and straightforward techniques for managing the challenges created by high-speed drivers

- EMI issues at the PCB, enclosure, and system level can be studied and visualized with sophisticated CEM tools. CEM facilitates the study of EMI design tradeoffs related to models and net design.

- Logic Design Engineers use time domain concepts. EMI Engineers use frequency domain concepts. Both need to communicate in each other's language.